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Ultrasonic Cleaning of Single-sided Printed Wiring Boards

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Printed wiring boards can be effectively cleaned after soldering by immersion in an ultrasonically agitated fluid. However, if semiconductor devices mounted on the board are also immersed, a significant number of the devices may develop electrical or mechanical faults.

"Kiss cleaning" (that is, application of the agitated fluid to only one side of the board, with the semiconductor devices in free air) is, with a suitable energy level and minimum effective cleaning time, substantially non-destructive. Kiss cleaning can be incorporated in a mechanical flow-solder production line.

The destructive nature of immersion cleaning is illustrated. A practical kiss cleaning specification (125W average ultrasonic power for 20 seconds) is given.

INTRODUCTION

Since 1963, several experiments have been carried out to determine the effect on semiconductor devices of ultrasonic energy. This investigation was in response to the desire of many users of electrical components to employ the thorough cleaning action of ultrasonic energy for removing solder flux residues from assembled printed wiring boards.

Initial proposals for cleaning boards involved total immersion of boards and components into an ultrasonically agitated organic solvent, hence this mode of cleaning was used in the first experiments. In a later experiment, only the undersides of boards were in contact with the agitated cleaning fluid, and it was shown that this technique, known as "kiss cleaning" (Ref. 1), was not likely to damage semiconductor devices.

EXPERIMENTS

Three experimental ultrasonic cleaning schedules have been investigated:

Experiment 1:	immersion, 500W peak, 125W average, 38 to 43kHz, several boards placed horizontally
Experiment 2:	immersion, 500W peak, 125W average, 38 to 43kHz, one board placed vertically
Experiment 3:	kiss cleaning, 450W peak, 112W average, 38 to 43kHz, one board placed horizontally at fluid surface.

Plainly, these experiments were neither exhaustive nor strictly comparable. Nevertheless, the results show that (1) and (2) destroy semiconductor devices, while (3) does not.

Experiment 1

In the first experiment an M.E.L. ultrasonic generator type L364 was used with a Kerry Ultrasonics type K142 tank. The energy developed was 500W peak, 125W average at a frequency of 38 to 43kHz. The fluid used was Arcton 113. The generator was tuned to give maximum agitation of the fluid.

Printed wiring boards carrying 285 point-contact diodes type OA95 were stacked horizontally in the tank and subjected to twelve successive 2min periods of cleaning.

Electrical measurements were made on the diodes before immersion and after each cleaning period. The results are given in Table 1.

The first catastrophic failures (two open-circuits) occurred after a total of 14min. After 24min, a total of sixteen catastrophic failures had occurred. Of these, ten were open-circuit and six were intermittent open-circuit.

Electrical failures (defined as more than 10% change in forward or reverse resistance) occurred after 2min (3 diodes), 4min (2 diodes), 10min (1 diode)—6 electrical failures in all.

Experiment 2

In the second experiment an M.E.L. generator type L364 was used with an M.E.L. type L368 tank. Again, the energy developed was 500W peak, 125W average at a frequency of 38 to 43kHz. The fluid used was Arcton 113. The generator was tuned to give maximum agitation of the fluid.

Printed wiring boards carrying 975 transistors or semiconductor diodes of 31 different types were immersed individually in the vertical plane. The bottom edge of the board was within 0·5in of the bottom of the tank, and the top edge was 0·5in below the fluid surface. The boards were subjected to 1min of cleaning and then (after retest of the semiconductor devices) to a further 2min.

Test results are shown in Table 2.

Eight types of device showed failures after 1min, and a further five showed failures after the additional 2min. The remaining eighteen types developed no faults. The mechanical failures were open-circuits; electrical failure was defined as a change of more than 10% in forward voltage at a current of 0·5mA. For transistors, both emitter-base and collector-base diodes were measured.

The semiconductor devices tested were chosen as being representative of present or recent mechanical designs. They are not necessarily preferred types for new equipment.

Experiment 3

In the third experiment a Headland Electrosonic type H120 generator was used with a 6in × 8in × 9½in deep tank. The energy developed was 450W peak, 112W average at a frequency of 38 to 43kHz. The fluid was Arcton 113. The generator was tuned to give maximum agitation of the fluid.

Printed wiring boards carrying 845 transistors or semiconductor diodes of 34 different types (chosen to represent the entire range of internal bond types and constructions likely to be most susceptible to damage by ultrasonic energy) were exposed, one at a time, horizontally, to the surface of the agitated fluid. Initial trials revealed that adequate cleaning of the flux-contaminated surface of the boards was achieved in 20s. The times subsequently used to determine the destructive effects of the technique were in the range 20s to 90s.

Results are shown in Table 3.

There was only one catastrophic failure. Only two devices out of 845 showed changes of more than 10% in forward voltage at 0·5mA. One was a 277OC with a 37% decrease in the forward voltage of the emitter-base diode; the other was an OC81 with a 20% decrease in the forward voltages of both diodes.

TABLE 1

Experiment 1 (Immersion cleaning)

285 point-contact diodes type OA95

Time (min)	Electrical failures	Mechanical failures
2	3	–
4	2	–
10	1	–
14	–	2
16	–	3
18	–	3
20	–	3
22	–	2
24	–	3
Total	6	16

TABLE 2

Experiment 2 (Immersion cleaning)

975 transistors or diodes of 31 types

Type	No. of samples	Failures after 1min Electrical	Failures after 1min Mechanical	Total failures after 3min Electrical	Total failures after 3min Mechanical
AAZ12	25	–	–	–	–
ACY17	25	–	1	–	1
AF117	25	–	–	–	–
AF180	25	–	–	–	1
AF186	25	–	–	–	–
AFY19	25	–	5	–	10
AFZ12	25	–	–	–	–
ASY67	25	–	–	–	1
ASZ21	25	–	–	–	–
BCY30	25	–	–	–	–
BCY38	25	–	–	–	–
BSY39	25	–	–	–	–
BY100	25	–	–	–	–
GET872	25	–	1	–	5
OA5	25	–	–	–	–
OA10	25	–	–	–	1
OA47	125	2	1	3	1
OA81	125	15	3	19	6
OA91	25	–	–	–	–
OA202	25	–	–	–	–
OAZ201	25	–	–	–	1
OAZ240	25	–	–	–	–
OC45	25	–	–	–	2
OC71	25	–	–	–	–
OC72	25	–	1	–	1
OC81	25	–	–	–	–
OC200	25	–	–	–	–
OC204	25	–	–	–	–
SX632	25	–	–	–	–
SX643	25	–	3	–	8
277OC*	25	–	1	–	1
Total	975	17	16	22	39

**Development type*

TABLE 3

Experiment 3 (Kiss cleaning)

845 transistors or diodes of 34 types

Type	No. of samples	Time (s)	Electrical failures	Mechanical failures
AAZ12	25	20	–	–
ACY17	25	20	–	–
AF117	25	90	–	–
AF180	25	90	–	–
AF186	25	20	–	–
AFY19	25	30	–	–
AFZ12	25	20	–	–
ASY67	25	20	–	–
ASZ21	25	60	–	–
BCY30	25	20	–	–
BCY38	25	60	–	–
BSY39	25	90	–	–
BY100	20	20	–	–
GET872	25	90	–	–
OA5	25	20	–	–
OA10	25	20	–	–
OA47	25	20	–	–
OA81	25	90	–	–
OA91	25	60	–	–
OA202	25	90	–	–
OAZ201	25	20	–	–
OAZ240	25	20	–	–
OC29	25	60	–	–
OC45	25	20	–	–
OC71	25	20	–	–
OC72	25	20	–	–
OC81	25	90	1	–
OC200	25	60	–	–
OC204	25	90	–	–
SX51	25	90	–	1
SX632	25	20	–	–
SX643	25	90	–	–
2N1302	25	90	–	–
277OC*	25	90	1	–
Total	845		2	1

**Development type*

CONCLUSIONS

The experiments were not designed in relationship to one another, but were performed at different times and in different places to meet particular needs. It is possible that a more exhaustive investigation would show that immersion cleaning could be rendered relatively non-destructive by adjustment of power levels or cleaning times. The experiments as performed, however, did produce an unacceptable proportion of failures, almost certainly attributable to the direct application of ultrasonic energy to the semiconductor devices.

Kiss cleaning, as performed in the third experiment, is shown to be substantially non-destructive, with only 0·35% of failures. A useful comparison can be made between the test results on types GET872, OA81, and SX643 in Tables 2 and 3. These types suffered damage by the immersion technique during 60s exposure, but none during kiss cleaning, even though the exposure time was extended to 90s.

At least one electronic equipment manufacturer has used kiss cleaning, as specified in experiment 3, for over six months without experiencing semiconductor device failure attributable to the process.

Ultrasonic power levels for different tanks, generators, and cleaning fluids are difficult to predict. However, it is considered that with any of the tanks and generators used in these experiments, a suitably designed kiss cleaning process will protect semiconductor devices from failure, whilst enabling the equipment manufacturer to exploit the unique cleaning characteristics of ultrasonic energy.

SPECIFICATION

The following is a sample specification for a kiss cleaning stage that can be installed immediately after a flow-solder stage in a printed wiring board production line.

Tank and Fluid	
Size:	15×20×24cm deep
Fluid:	Methylated spirit, Arcton 113, or any suitable fluid of a comparable viscosity (The harmful effects of certain non-recommended fluids are discussed in Ref. 1)
Fluid depth:	20cm
Generator	
Peak power:	500W max
Average power:	125W approx
Frequency:	38 to 43kHz
Cleaning schedule	
Time:	20s

This specification should give adequate cleaning of all single-sided printed wiring boards, and should be safe for all semiconductor devices. The ultrasonic generators commercially available may need to be used with some degree of damping to restrict the ultrasonic energy to the specified level. Careful design and monitoring of the ultrasonic system are desirable.

REFERENCE

Byrd, G. C. M. and Clay, W. M. 'Safeguards for Transistors during Ultrasonic Cleaning.' **Ultrasonics**, Oct. 1966, pp. 195 to 198.

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pages 82 and 87, Figs. 7 and 11

The asymmetrical voltage dependent resistor VDR_1 should have its cathode (marked 'k') connected to the line joining terminal 17 to R_3, and its anode connected to R_{47}, R_{26}, etc.

page 82,

The value of R_3 should be 33Ω.

page 99, right hand column

In the instructions for setting resistors, the first instruction should read,

(i) Set R_{15} with its slider at the end nearer to terminal 19.

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page 112

In Fig. 3 there should be no direct connection between Phase Comparator and Sub-carrier Phase Switch.

page 123

In Fig. 9 the changeover switch to the right of TR_4 is wrongly annotated. The upper contact should be marked '625', and the lower '405'.

Dual-standard Vision and Sound I.F. Amplifiers for Monochrome and Colour Signals

G. D. Browne and L. Fahidy
Mullard Central Application Laboratory

An unneutralised dual-standard vision i.f. amplifier using BF167 and BF173 low-feedback transistors with simply-constructed, single-tuned-circuit interstage couplings is described. The design uses stagger-tuning for the first and second stages and a low Q-factor broadband output. It avoids the difficulties associated with bandpass transformers, has considerable flexibility, and is easy to align.

By adjustment of the tuning of the first and second stages, the 405-line and 625-line vision carriers can be set quite easily and independently to their −6dB points relative to midband. This produces negligible change to the top of the overall response curve which, if desired or necessary, can be tilted by a small adjustment of the output coil.

Use of a phase splitter after the video detector enables a higher load resistance to be used, simplifies system switching, minimises harmonic distortion, and accommodates a simple chrominance filter.

The two-stage sound i.f. amplifier uses BF194 transistors. During 405-line operation, a.g.c. is applied directly to the first stage from the detector; during 625-line operation, the output stage acts as a limiting amplifier.

INTRODUCTION

In many television receiver designs, the overall gain attainable with a three-stage vision i.f. amplifier (80 to 90dB with BF167 and BF173 silicon planar transistors, for example) may be higher than is necessary. Consequently, the transistor characteristics can be better exploited by using a coil construction that leads to improved reproducibility at the expense of gain. In the amplifier described here, BF167 and BF173 transistors are used in unneutralised stages, and some gain has been sacrificed to obtain better reproducibility.

The sound i.f. amplifier needs only two stages. Because the gain per stage is lower than in the vision amplifier, good stability is readily achieved with BF194 transistors (which have a higher feedback capacitance than the BF167 and BF173).

One essential requirement of an i.f. amplifier intended for use in a colour television receiver is stability of response with changing a.g.c. signal. A change in the response of the vision carrier relative to the chrominance subcarrier should not be greater than about ±1dB. To achieve this degree of stability, a slight sacrifice of gain in the controlled stage appears inevitable. In other respects, an amplifier design using the normal techniques of monochrome television appears to be entirely satisfactory for a PAL-D receiver.

The use of a single detector to provide luminance, chrominance, and intercarrier f.m. sound is known to produce intermodulation beats between the chrominance and sound signals. These beats can be prevented effectively either by the use of separate detectors or by attenuating the sound carrier by about 36dB relative to the chrominance carrier.

Tests indicate that it is possible to produce a single detector amplifier that is adequate for all but very sophisticated receivers. In the design described here, a single detector arrangement is used.

TUNED-CIRCUIT CONSIDERATIONS

Although theoretically advantageous because of improved selectivity, the use of bandpass interstage coupling entails a number of practical difficulties. In general, bandpass transformers must operate with a relatively low working Q-factor and have to be critically coupled or nearly critically coupled. This leads to the necessity of providing sufficiently close coupling. The use of mutual inductance would give the most satisfactory results, but the spacing between primary and secondary windings then becomes very small—even commensurate with the wire diameter. Apart from the obvious difficulties of maintaining such spacing, the proximity of the tuning slugs introduces an additional and variable factor. Other methods of coupling can become complicated and are likely to require separate cans for primary and secondary windings. These remarks are especially valid in connection with the vision output stage.

An alternative approach is to use single-tuned circuits. No selectivity problem then arises in the output stage because this is always wideband. The intermediate stage couplings can be relatively narrow band and stagger-tuned to provide correct overall response. A bandpass transformer is used as a coupling arrangement between the amplifier and the tuner, however, to allow convenient separation of the units. The circuit of the complete amplifier is shown in Fig. 1.

A single detector arrangement provides the luminance, chrominance, and intercarrier f.m. sound outputs. The use of a phase splitter following the video output circuit makes a detector polarity-reversing switch unnecessary.

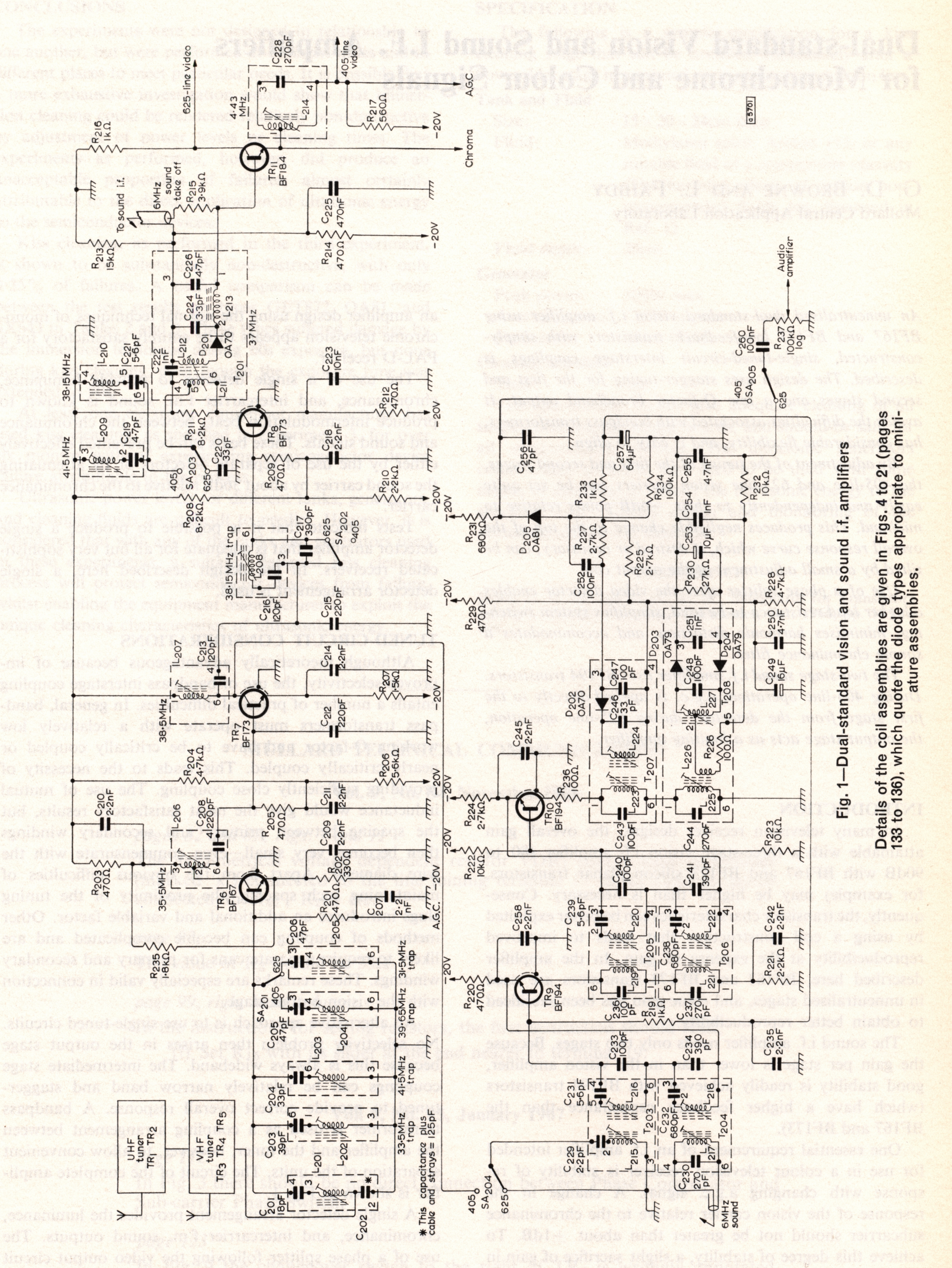

Fig. 1—Dual-standard vision and sound i.f. amplifiers

Details of the coil assemblies are given in Figs. 4 to 21 (pages 133 to 136), which quote the diode types appropriate to miniature assemblies.

Also, because of its relatively low input capacitance, the phase splitter enables a higher value of diode load to be used, thus giving better linearity and a greater voltage output.

VISION AMPLIFIER

The response of the vision amplifier is defined at the −6dB points almost entirely by the characteristics of the output and other interstage couplings. Two permanent traps at the amplifier input provide a skirt rejection of about 40dB, and serve to augment the basic attenuation. One trap operates at 33·5MHz (625-line sound and, approximately, 405-line adjacent sound) and the other at 41·5MHz (625-line adjacent sound and channel 1 sound).

Output Stage

The output stage, TR_8, uses a BF173 transistor operating at 16·5V, 7mA (115mW) from a −20V supply and has a Q-factor of approximately 4. The inductance, L_{211}, is tuned by the transistor output capacitance to a midband frequency of approximately 37MHz. To provide d.c. isolation for the diode and its load, the secondary is bifilar-wound with the primary.

With a 3·9kΩ diode load, the resistance reflected into the secondary is, after allowing for the rectification efficiency, about 2·5kΩ, which is approximately the collector load for maximum power output. Hence, the primary and secondary windings have the same number of turns, which minimises the leakage inductance. (To prevent the Q-factor rising too much on low-level signals because of the reduced rectification efficiency, a shunt resistor of 8·2kΩ is connected across the primary winding). A π-type h.f. filter ensures adequate filtering and allows a relatively small input capacitance to be used, thereby minimising the change in reflected tuning capacitance and reducing phase modulation to a minimum. The primary winding is tapped to allow the inclusion of two traps operating at 41·5MHz (channel 1 sound) and 38·15MHz (405-line sound i.f.). Each trap contributes 14 to 16dB attenuation during 405-line operation. Their absence during 625-line operation is compensated for by switching in a small capacitor, C_{220}. The lead length of this capacitor must be kept short to avoid unwanted self-resonance in the passband; this self-resonance causes a dimple or trough in the overall response.

It is important that the tuning slug for the output inductor, L_{212}, should be in the earthy (tapped) end of the coil to reduce leakage inductance in the trap circuit.

Second Stage

To obtain good signal-handling capacity, the second i.f. stage, TR_7, also uses a BF173, which operates at 10V, 7mA (70mW). The collector load comprises a single-tuned capacitively-tapped circuit feeding the base of the output stage. The operating Q-factor is about 20, and the circuit is tuned to approximately 38·5MHz.

For 405-line operation, a shunt-tuned capacitively-tapped trap is switched in to attenuate the 38·15MHz sound i.f. signal by 20dB. A sound take-off circuit that provides 6dB attenuation of the vision signal is fed from the collector. The total 38·15MHz rejection just exceeds 40dB. This could be increased, but with simple traps having a Q-factor not exceeding 100 their presence would encroach too far into the vision band.

First Stage

The first stage, TR_6, uses a BF167 which is designed to have a forward gain control characteristic with maximum gain occurring at a collector current of about 4mA. At a current of 13mA, the gain is reduced by 40dB. Care has been taken to avoid exceeding the permitted dissipation.

Because of large changes in transistor parameters over this current range, the collector is tapped in close to the earthy end of the coil, which provides the other half of the stagger-tuned pair referred to (p.129), and is tuned to 35·5MHz. The operating Q-factor of about 20 is determined very largely by the capacitive tap and the input impedance of the second stage. This arrangement reduces changes in the Q-factor and response curve with a.g.c. to an acceptable level. The a.g.c. drive is applied to the base of the BF167 in the usual manner, and variations in transistors are automatically compensated for during alignment.

Tuner-I.F. Coupling

The i.f. output from the tuner is coupled to the input of the i.f. amplifier by means of a bottom-capacitance-coupled broadband transformer. The primary is in the tuner itself and the secondary in the i.f. amplifier. The secondary is capacitively tapped into the base of the first stage so as to minimise the effects of changes in transistor parameters over the range of gain control.

The tuner and i.f. amplifier are connected together by means of a co-axial cable which provides some of the bandpass coupling capacitance. Although this arrangement gives a desirable mechanical flexibility, it is prudent to keep the link short relative to a quarter-wavelength at 37MHz; that is, the link should not generally exceed 60cm when it will contribute not more than 40 to 45pF of the coupling capacitance required (approximately 120pF total).

This stage of the amplifier also incorporates four traps. The two at 33·5 and 41·5MHz that have already been discussed are permanently in circuit; a third trap, at 31·5MHz (adjacent vision), is switched in for 625-line operation only; and a fourth, at 39·65MHz (adjacent vision), is switched in for 405-line operation only.

SOUND AMPLIFIER

The sound i.f. amplifier is a dual-standard two-stage arrangement using BF194 transistors. The first stage, TR_9, has its two inputs (at 38·15 and 6MHz) connected in series, and provision is made for application of a.g.c. to the base of the transistor. The collector circuit of the second stage, TR_{10}, has the primary winding of the a.m. detector circuit in series with the primary winding of the ratio detector so as to avoid unnecessary switching.

To obtain the best possible signal-to-noise ratio, the a.m. input to the sound amplifier is short-circuited during f.m. operation for 625-line signals, and the selection of the relevant a.f. output is achieved by means of a simple change-over switch (SA_{204}). During 625-line operation—that is, in the absence of a 38·15MHz a.m. sound carrier—no a.g.c. voltage is produced. Under these conditions, the amplifier operates at maximum gain and has a limiting action on the 6MHz sound signals. During 405-line operation, normal a.g.c. conditions control the level of the 38·15MHz a.m. sound carrier at its detector. A conventional rate-of-rise noise-limiting diode, D_{205}, is included in the audio output. The circuit diagram of the complete amplifier is shown in Fig. 1.

PERFORMANCE

Response

During 625-line operation, the main vision amplifier has a 6dB bandwidth of about 5MHz; under 405-line conditions, it is approximately half this value. Typical response curves are shown in Figs. 2 and 3. The sound amplifier has a 6dB bandwidth of 750kHz for the 38·15MHz a.m. carrier, and the discriminator is linear to about ±100kHz for the 6MHz f.m. signal.

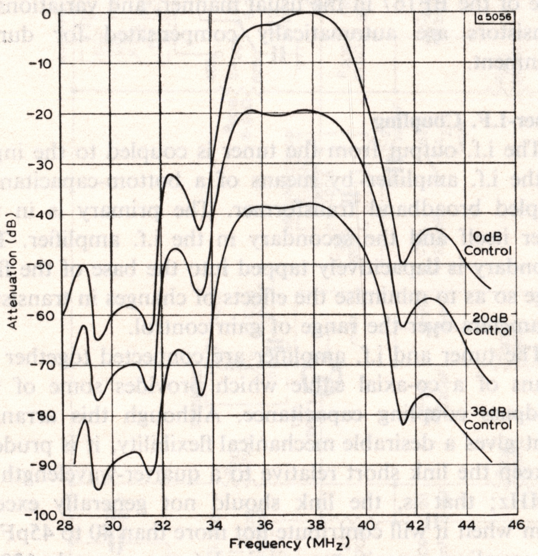

Fig. 2—Typical response curve for 625-line operation

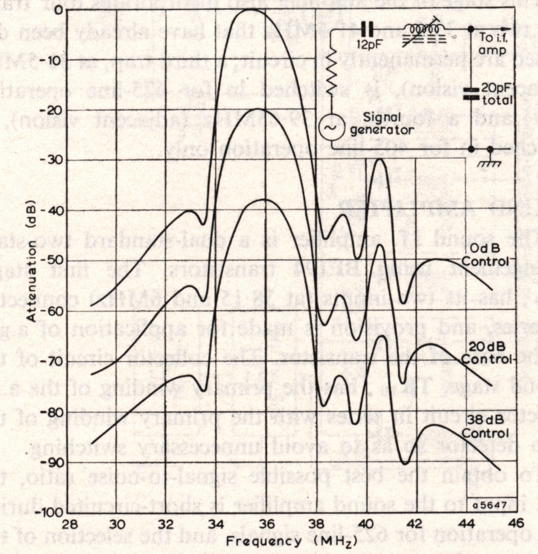

Fig. 3—Typical response curve for 405-line operation

Sensitivity

The sensitivity of the vision i.f. amplifier is conveniently expressed in terms of the voltage (r.m.s.) at the transistor bases (midband frequency) required to produce 2V d.c. at the video detector.*

At the base of the last transistor, the figure is about 20mV (corresponding to a power gain of nearly 30dB), at the second base, 1mV(26dB), and at the first base about 150µV (14dB). The last figure is somewhat less than might be desired because of the degree of mismatch required with this tuned circuit to minimise distortion of the overall response curve resulting from a.g.c. action. The variation in the relative level of the vision and chrominance carriers does not exceed ±1dB over the 40dB control range. Such considerations are of vital importance in a colour receiver.

A typical u.h.f. tuner gain is 28dB (either a u.h.f. tuner feeding into a v.h.f. tuner or an integrated type with some i.f. gain). With allowance for 6dB loss for part of the coupling network and the associated trap circuits, the overall receiver midband sensitivity is 20 to 25µV e.m.f. for 2V d.c. at the video detector. These figures have been confirmed by measurement in receivers.

Signal Output

In the 625-line system, it is possible to obtain a black-to-white video signal of more than 4·5V before the onset of synchronising pulse compression. In the 405-line system also a black-to-white signal of 4·5V can be obtained before cramping of the white occurs.

Both f.m. and a.m. detector outputs are more than adequate to drive an audio amplifier, having a sensitivity of 100mV and an input resistance of not less than 25kΩ, for full output.

Stability

When the complete amplifier is correctly aligned, its stability is very high. Numerically, the stability factor† for the first and last vision stages (both systems) and each sound stage exceeds 10 for 6MHz. The figure for the second vision stage (both systems) and the two sound stages is greater than 5 for 38·15MHz.

These stability factors have been established in a complete receiver operating at maximum gain by increasing the feedback capacitance with added capacitance until noticeable distortion of the signal occurred.

COIL SPECIFICATIONS

The component designations used in Fig. 1 all have standard type numbers or values. Certain diodes associated with miniature coil assemblies, however, are subminiature types and have different type numbers.

The details of the wound components and the subminiature diode type numbers used in the miniature coil assemblies are shown in Figs. 4 to 21. All these figures show underside views.

---

*2V d.c. at midband frequency corresponds to 1V at the vision carrier frequency.

†The stability factor S is defined as

$$S = (C+C_{\text{added}})/C$$

where C is the total existing feedback capacitance.

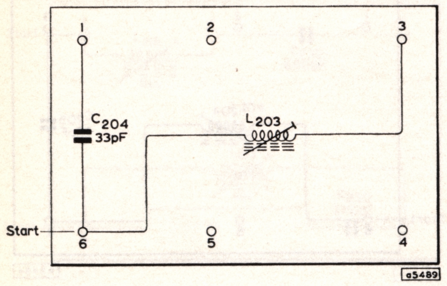

Fig. 4—41·5MHz input trap

Assembly Components

Former:	P1011/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/short	Brayhead
Screw core:	4×0·5×6/900 (Small assembly)	Neosid

11 turns, 24 s.w.g. en.cu.wire

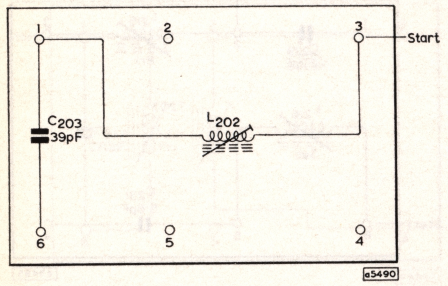

Fig. 5—33·5MHz input trap

Assembly Components

Former:	P1011/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/short	Brayhead
Screw core:	4×0·5×6/900 (Small assembly)	Neosid

14 turns, 24 s.w.g. en.cu.wire

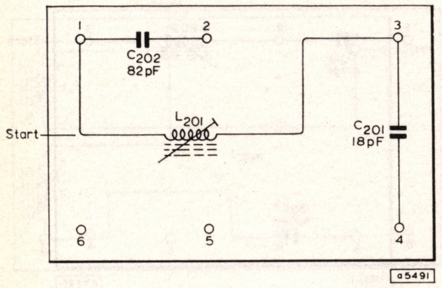

Fig. 6—Input to vision i.f. amplifier

Assembly Components

Former:	P1011/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/short	Brayhead
Screw core:	4×0·5×6/900 (Small assembly)	Neosid

15 turns, 30 s.w.g. en.cu.wire

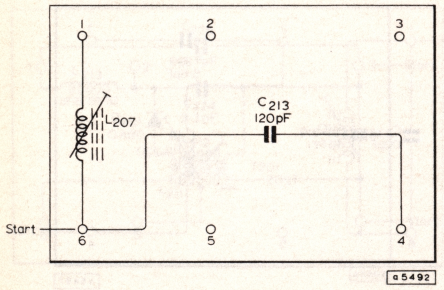

Fig. 7—Collector load of second stage

Assembly Components

Former:	P1011/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/short	Brayhead
Screw core:	4×0·5×6/900 (Small assembly)	Neosid

5½ turns, 24 s.w.g. en.cu.wire

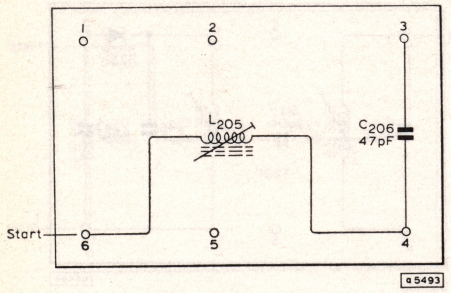

Fig. 8—31·5MHz input trap

Assembly Components

Former:	P1011/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/short	Brayhead
Screw core:	4×0·5×6/900 (Small assembly)	Neosid

14 turns, 24 s.w.g. en.cu.wire

Assembly Components
Former: P10011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
Screw core: 4×0·5×6/900 Neosid
(Small assembly)
7 turns, 24 s.w.g. en.cu.wire

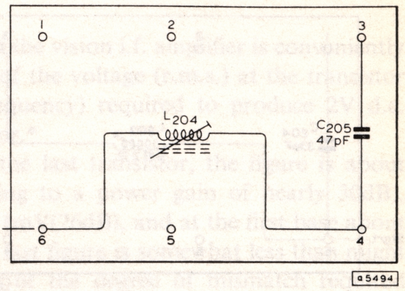
1
2
3
L204
C205
47pF
Start
6
5
4
a5494

Fig. 9—39·65MHz input trap

Assembly Components
Former: P1011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
2 screw cores: 4×0·5×6/900 Neosid
(Small assembly, primary coil on bottom of bobbin)
Primary: 35 turns, 40 s.w.g. en.cu.wire
Spacing: 5mm
Secondary: 20 turns, 40 s.w.g. en.cu.wire

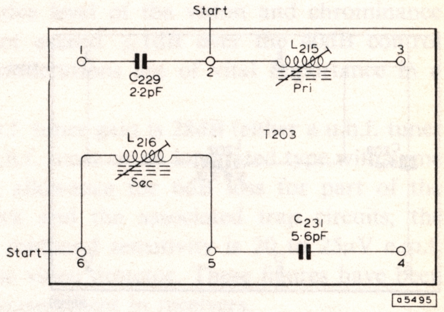
Start
1
C229
2·2pF
2
L215
Pri
3
L216
Sec
T203
C231
5·6pF
Start
6
5
4
a5495

Fig. 10—38·15MHz trap and sound take-off

Assembly Components
Former: P1011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
Screw core: 4×0·5×6/900 Neosid
(Small assembly)
33 turns, 30 s.w.g. en.cu.wire

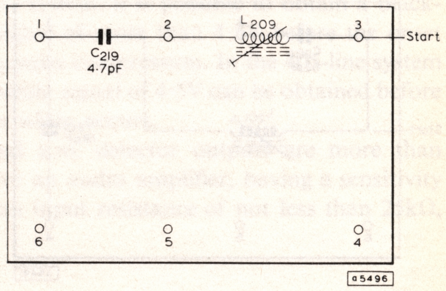
1
C219
4·7pF
2
L209
3
Start
6
5
4
a5496

Fig. 11—41·5MHz output trap

Assembly Components
Former: P1011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
2 screw cores: 4×0·5×6/900 Neosid
(Small assembly, primary coil on bottom of bobbin)
Primary: 4 turns, 30 s.w.g. en.cu.wire
Spacing: 5mm
Secondary: 21 turns, 40 s.w.g. en.cu.wire

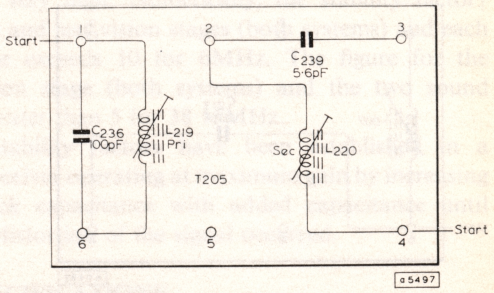
Start
1
2
C239
5·6pF
3
C236
100pF
L219
Pri
Sec
L220
T205
6
5
4
Start
a5497

Fig. 12—A.M. i.f. transformer

Assembly Components
Former: P1003/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/long Brayhead
2 screw cores: 4×0·5×6/900 Neosid
(Large assembly, primary coil on bottom of bobbin)
Primary: 4 turns, 30 s.w.g. en.cu.wire
Spacing: 4·5mm
Secondary: 9 turns, 30 s.w.g. en.cu.wire

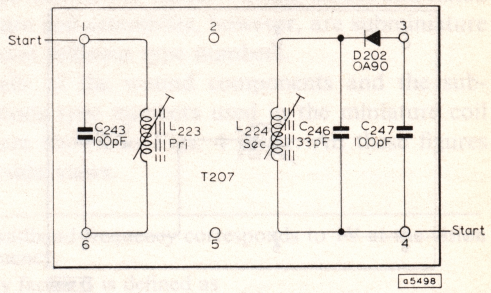
Start
1
2
3
D202
OA90
C243
100pF
L223
Pri
L224
Sec
C246
33pF
C247
100pF
T207
6
5
4
Start
a5498

Fig. 13—A.M. detector

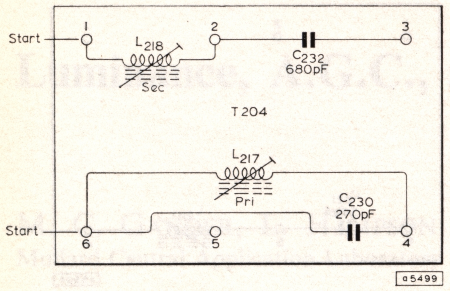
Start
1
L218
Sec
2
C232
680pF
3
T204
L217
Pri
C230
270pF
Start
6
5
4
a5499

Fig. 14—6MHz sound take-off

Assembly Components
Former: P1011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
2 screw cores: 4×0·5×6/900 Neosid
(Small assembly, primary coil on bottom of bobbin)
Primary: 22 turns, 40 s.w.g. en.cu.wire
Spacing: 3·5mm
Secondary: 22 turns, 40 s.w.g. en.cu.wire

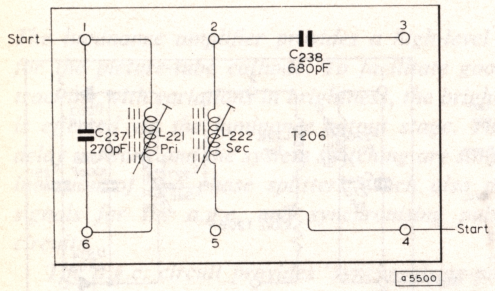
Start
1
2
C238
680pF
3
C237
270pF
L221
Pri
L222
Sec
T206
6
5
4
Start
a5500

Fig. 15—F.M. i.f. transformer

Assembly Components
Former: P1011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
2 screw cores: 4×0·5×6/900 Neosid
(Small assembly, primary coil on bottom of bobbin)
Primary: 22 turns, 40 s.w.g. en.cu.wire
Spacing: 3·5mm
Secondary: 22 turns, 40 s.w.g. en.cu.wire

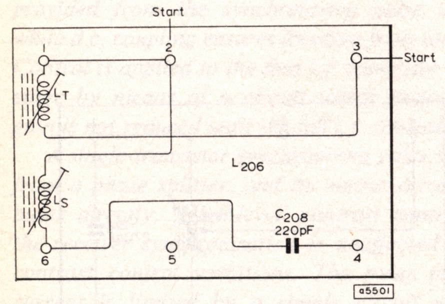
Start
1
2
3
Start
LT
L206
LS
C208
220pF
6
5
4
a5501

Fig. 16—Collector load of first stage

Assembly Components
Former: P1011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
Screw core: 4×0·5×6/900 Neosid
(Small assembly, L_T on bottom of bobbin)
L_T, 1 turn, 24 s.w.g. en.cu.wire
L_S, 3 turns, 24 s.w.g. en.cu.wire

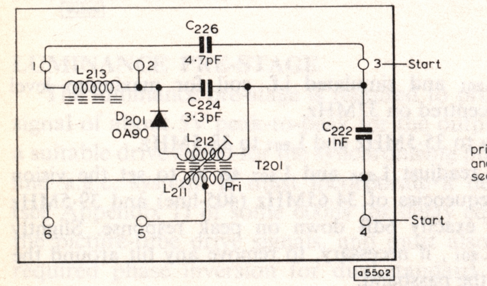
C226
4·7pF
1
L213
2
3
Start
C224
3·3pF
D201
OA90
L212
C222
1nF
T201
L211
Pri
6
5
4
Start
r.f.c.
pri.
and
sec.
a5076
a5502

Fig. 17—Vision output transformer

Assembly Components
Former: P1003/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/long Brayhead
Screw core: 4×0·5×12·7/900 Neosid
(Long assembly)
Primary and
Secondary: 25+25 turns, 38 s.w.g. en.cu.wire, bifilar wound. Primary tapped 3 turns from the start.
Core inserted from bottom of bobbin
R.F.C.: 75 turns, 44 s.w.g. en.cu.wire on dust iron former, Neosid CH2.

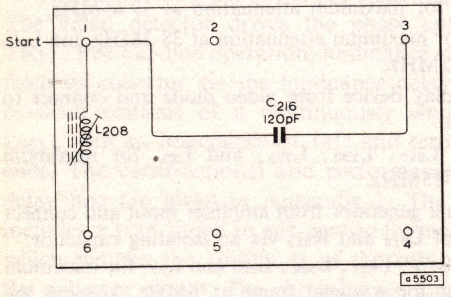
Start
1
2
3
L208
C216
120pF
6
5
4
a5503

Fig. 18—38·15MHz intermediate trap

Assembly Components
Former: P1011/1 Brayhead
Terminal base: P1001 Brayhead
Can: P5000/short Brayhead
Screw core: 4×0·5×6/900 Neosid
(Small assembly)
5 turns, 24 s.w.g. en.cu.wire

Assembly Components

Former:	P1011/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/short	Brayhead
Screw core:	4×0·5×6/900	Neosid

(Small assembly)

33 turns, 30 s.w.g. en.cu.wire

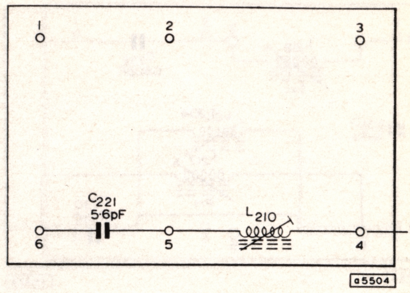

Fig. 19—38·15MHz output trap

Assembly Components

Former:	P1003/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/long	Brayhead
Screw core (primary):	4×0·5×6/900	Neosid
Screw core (secondary):	4×0·5×12·7/900	Neosid

(Large assembly)

Primary:	18 turns, 40 s.w.g. en.cu.wire
Tertiary:	12 turns, 40 s.w.g. en.cu.wire
Spacing:	2·5mm
Secondary:	2×25 turns, 42 s.w.g. en.cu.wire bifilar wound, turns spaced by wire diameter.

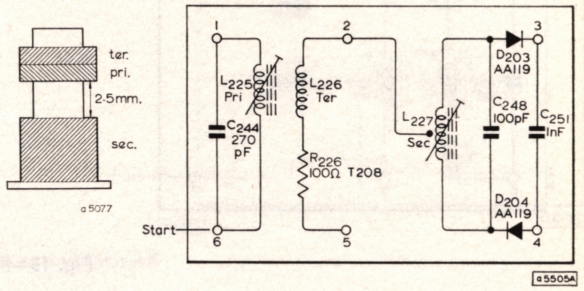

Fig. 20—Ratio detector

Assembly Components

Former:	P1011/1	Brayhead
Terminal base:	P1001	Brayhead
Can:	P5000/short	Brayhead
Screw core:	4×0·5×6/900	Neosid

(Small assembly)

36 turns, 38 s.w.g. en.cu.wire, centre-tapped

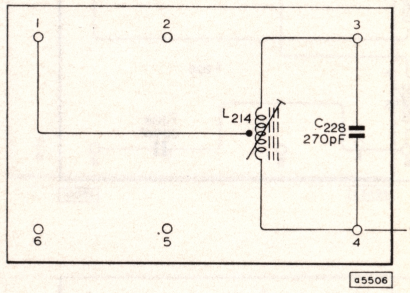

Fig. 21—Chrominance filter

APPENDIX

Alignment Procedure

1. Provide a suitable circuit to simulate the i.f. coil in a typical tuner (see inset on Fig. 3 for suggested circuit).
2. Wire in a manual gain control arrangement (for example, battery and potentiometer).
3. Switch to 625-line position.
4. Disconnect signal input from base of TR_8 and apply, through an isolating capacitor (1000pF), a swept calibrated oscillator (for example, Polyskop). Tune L_{201} to 37MHz using an input level to produce 2V d.c. across the video diode load R_{215}.
5. Switch to 405-line position.
6. Adjust traps L_{209} and L_{210} for maximum attenuation at 41·5MHz and 38·3MHz respectively.
7. Switch to 625-line position.
8. Remove signal generator from base of TR_8 and reinstate normal connection.
9. Apply signal generator to simulated tuner i.f. coil.
10. Adjust L_{202}, L_{203} and L_{205} for maximum attenuation at 33·5MHz, 41·5MHz and 31·5MHz respectively.
11. Set manual gain control to give 20dB down on full amplifier gain.
12. Adjust L_{201} and simulated i.f. coil for maximum level response centred on 37MHz.
13. Tune L_{206} to 35·5MHz and L_{207} to 38·5MHz.
14. Carefully readjust L_{206} and L_{207} so as to set the vision carrier frequencies of 34·65MHz (405-line) and 39·5MHz (625-line) exactly 6dB down on peak response. Slightly readjust L_{201}, if necessary, to remove any tilt around the centre of the passband.
15. Repeat operations 12, 13 and 14 if necessary.
16. Switch to 405-line position.
17. Adjust L_{204} for maximum attenuation at 39·65MHz.
18. Tune L_{208} for maximum attenuation at 38·3MHz and L_{215} to about 38·2MHz.
19. Remove display device from video diode and connect to audio output.
20. Tune L_{216}, L_{219}, L_{220}, L_{223}, and L_{224} for maximum output at 38·15MHz.
21. Remove signal generator from amplifier input and connect to junction of L_{213} and R_{215} via an isolating capacitor.
22. Tune L_{217}, L_{218}, L_{221}, L_{222}, L_{225} and L_{227} for maximum audio output for a signal input at 6MHz, keeping the level sufficiently low to avoid limiting action.

Luminance, A.G.C., and Sync Circuits for PAL-D Receivers*

M. C. GANDER, L. HAMPSON AND D. S. HOBBS
Mullard Central Application Laboratory

The luminance amplifier provides a high-level drive signal for the picture-tube cathode. To facilitate good grey-scale tracking with variations in brightness, the brightness control is effected via the luminance output stage. The luminance delay network and the system switching are simplified by the inclusion of two phase splitters which also provide drive signals for the a.g.c. and synchronising pulse separator circuits.

The a.g.c. circuit provides 'synchronising-pulse-tip' control for 625-line operation and 'back-porch' control for 405-line operation. Gating action for 405-line operation is provided from the synchronising pulse separator circuit, while d.c. coupling ensures freedom from lock-out conditions. Control is applied to the first i.f. transistor and the tuner r.f. stage by means of a circuit which ensures that the tuner gain is not reduced until the full i.f. control has been applied.

A single-transistor synchronising pulse separator is driven from a phase splitter, and its output drives the valve timebases directly. 'High-level' contrast control is used, hence the receiver synchronisation is unaffected by brightness or contrast control variations. The mean picture tube beam current is limited by a simple circuit which reduces the effect on the picture of maladjustment of the brightness or contrast controls.

LUMINANCE PRE-STAGE

The luminance pre-stage is required to provide a video signal of about 5V peak-to-peak for the output stage, and a suitable drive signal for the synchronising pulse separator and a.g.c. system. It must incorporate a delay network (see Appendix 1) of some 600ns for delay equalisation of the picture-tube drive signals, and must also provide the required phase inversion for dual-standard operation.

Circuit Description

The circuit diagram of the pre-stage is shown in Fig. 1. The video detector drives the phase splitter transistor TR_{11}. For 625-line operation, luminance signals are taken from its collector via the luminance delay network. This network consists of a continuously wound delay line, L_{301}, with an impedance of 1kΩ and terminated at both ends. The constructional and performance details of the delay line are given in Appendix 1. The emitter circuit includes a trap tuned to sub-carrier frequency (4·43MHz) which reduces the amplitude of the sub-carrier signal in the collector circuit. The chrominance amplifier is driven from the emitter with a simple C–R filter network.

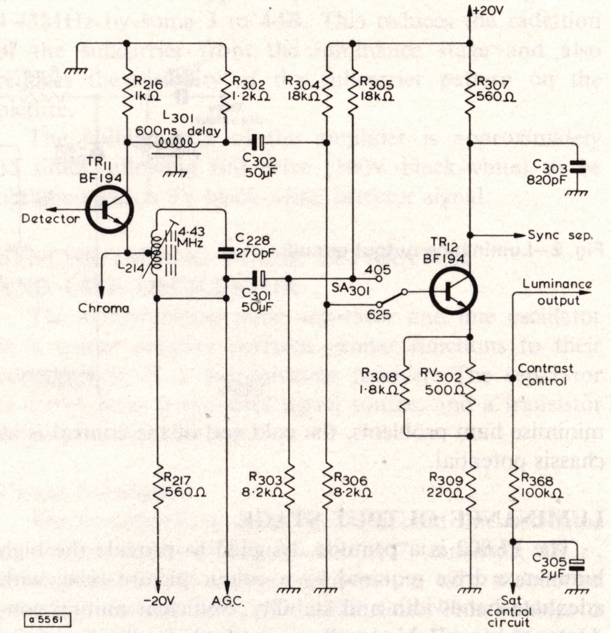

Fig. 1—Video pre-stage

For 405-line operation, the video signal is taken from the emitter to the system change-over switch. This switch is used to select a positive-going video signal for the output stage and hence obviates the need for switching in the detector circuit.

The drive for the a.g.c. system is also taken from the emitter of the phase splitter for both systems. This is a convenient low-impedance point where the output is positive-going for an increase in signal. The only system switching necessary is to enable a sampling pulse to be included for 405-line operation. This circuit is described in detail on page 141.

A low-impedance high-level contrast control is desirable since it enables the picture contrast to be varied independently of the synchronising and a.g.c. circuits. Furthermore, the termination of the luminance delay network is simplified if the capacitive load can be minimised. A second phase splitter TR_{12} is therefore used, with the synchronising pulse separator driven from its collector and the contrast control from its emitter. The control grid of the PL802 output valve is a.c. coupled from the slider of the contrast control with a d.c. restoring diode. To

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*These circuits are also suitable for PAL-S and NTSC receivers.

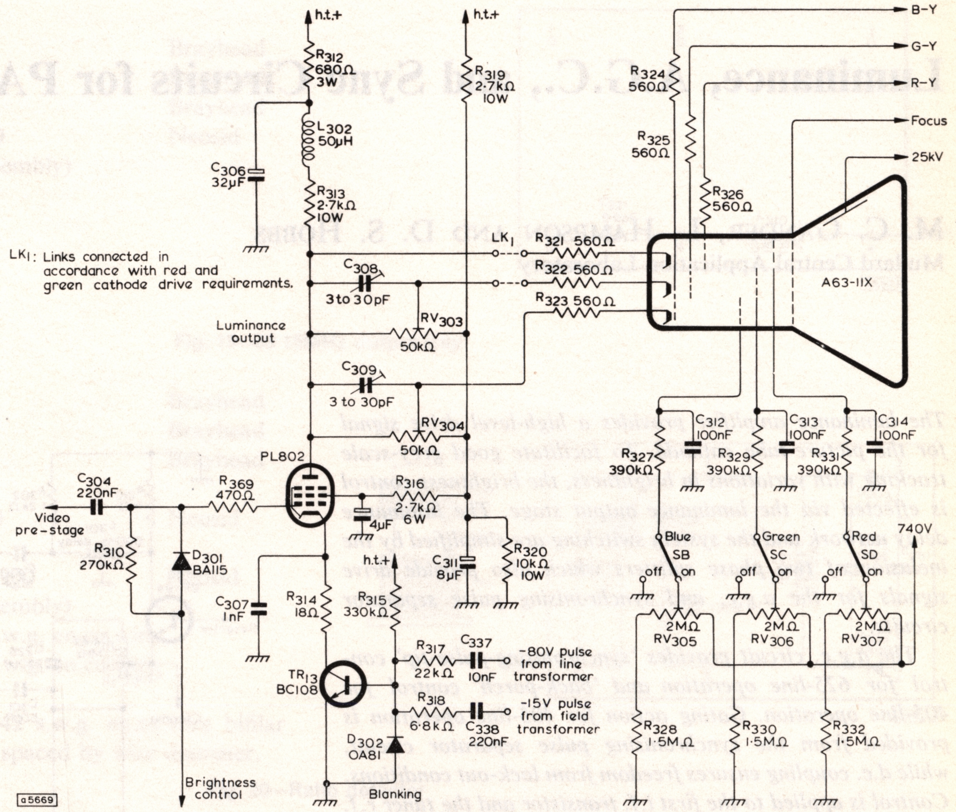

Fig. 2—Luminance output circuit

minimise hum problems, the cold end of the control is at chassis potential.

LUMINANCE OUTPUT STAGE

The PL802 is a pentode designed to provide the high luminance drive required by a colour picture tube, with adequate bandwidth and stability. Sufficient mutual conductance is available to allow a cathode feedback resistor to be employed; this resistor also raises the grid input impedance and reduces the gain spreads from valve to valve.

The rated peak current swing is sufficient to fully drive a colour tube with 100V black-white luminance voltage. This is equivalent to a total dynamic drive (including the synchronising pulse) of 140V across a 2·7kΩ anode load resistor. Brightness control through the luminance stage is effected by providing a 25V variation in d.c. level via the grid circuit d.c. restorer.

Potentiometer feed to the picture tube is achieved by two 50kΩ potentiometers (green and blue guns) and a fixed black-level reference divider between the h.t. supply line and chassis.

A decoupled anode load is used to obtain a large d.c. voltage swing without exceeding the anode dissipation rating. Compensation for the loss of d.c. component which would occur in the luminance signal is achieved in the screen-grid circuit, which introduces the desired amount of d.c. degeneration and also limits the possible screen-grid dissipation to a safe value. The a.c. and d.c. gains are equal to within ±10%, which appears to be adequate for good picture quality.

Blanking is applied by means of a series transistor, TR_{13}, in the cathode circuit. This allows low-level blanking pulses to be used where previously high voltages have been necessary for application to the first anode of the picture tube or to the luminance circuit.

Maladjustment of the brightness or contrast controls can result in severe overdrive of the picture tube, producing a loss of definition and contrast. To minimise such effects, some form of beam current limiting is required. The e.h.t. current is supplied by the line timebase, and a limiting circuit operated from the timebase is more convenient than one that monitors the tube current directly. The bias for the luminance stage is increased if the line timebase mean current exceeds a value predetermined by the limiting circuit.

Circuit Description

The luminance output stage is shown in Fig. 2. It has been designed to operate from a high-level contrast control potentiometer. A d.c. restoring diode D_{301} operating on synchronising pulse tips is used at the grid; brightness control is applied by varying the negative bias at the anode of the restoring diode.

The cathode circuit consists of a feedback resistor R_{314}, bypassed for h.f. compensation by C_{307}, and transistor TR_{13} which is used for blanking insertion. The transistor is bottomed by current through R_{315}. Negative blanking pulses of 80V at line frequency and 15V at field frequency are applied to the resistors R_{317} and R_{318} respectively to cut off the transistor; diode D_{302} prevents reverse breakdown of the base-emitter junction. The collector voltage at cut-off is limited to the grid cut-off voltage (approximately −10V) of the PL802.

The anode circuit of the luminance valve consists of a load resistor R_{313} (2·7kΩ), a peaking coil L_{302}, and a decoupling resistor R_{312}. These have been chosen to ensure that the anode dissipation rating is not exceeded when working from a nominal 285V h.t. line.

A potentiometer/potential divider network is used to feed the green and blue picture tube cathodes, while the red cathode is connected directly to the luminance valve anode. To achieve drive amplitude variations without d.c. level shift, the potentiometers are connected between the anode of the luminance valve and a fixed voltage divider between the 285V h.t. line and chassis. At black-level with a full drive signal, the anode voltage is 220V. Therefore both drive potentiometers are connected to the same tapping point on the potential divider. Small trimmer capacitors C_{308} and C_{309} connected across the drive potentiometers compensate for the loss of drive at the higher luminance frequencies.

The first anodes of the picture tube are supplied from the boost voltage of the line timebase by means of a resistor and smoothing capacitor (Ref. 1, Fig. 3.1). The range of first-anode voltage required is +220 to +520V, but since the cathodes are at +220V at black-level, a range of +440 to +740V is actually necessary. Operation of switches S_B, S_C and S_D removes the first-anode potentials: they need to be switched off for test and adjustment purposes (see Appendix 2). Spark gaps are connected between each electrode and the external coating of the picture tube, and are used in conjunction with isolating resistors to limit the effects of internal flashover.

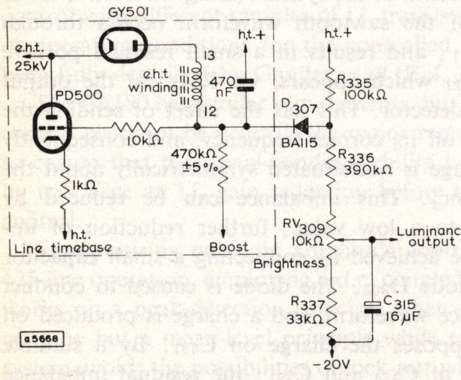

Fig. 3—Beam current limiting circuit

The beam-current limiting circuit (Fig. 3) is operated from the control-grid circuit of the shunt stabiliser in the line timebase (Ref. 1). Under normal picture conditions, the shunt stabiliser is conducting, and the catching diode D_{307} is normally non-conducting. As the mean beam current of the picture tube increases, the potential at the control grid of the shunt stabiliser becomes more negative. If the stabiliser is cut off, it ceases to regulate the e.h.t. current, and its control grid goes very negative, causing the catching diode to conduct. The diode is connected into the brightness control circuit, and the current through the diode reduces the potential across the brightness control, thus limiting the mean current of the picture tube.

Whenever the mean beam current is below the stabilised value set by the shunt regulator, this control technique will have no effect upon the operation of the receiver as the feedback loop is open. In the event of maladjustment of the brightness or contrast controls, or an excessive increase in the mean picture content, or any combination of these, the beam current is limited to its predetermined value. The loop gain of the limiting system is adequate since the brightness control is in the grid circuit of the luminance output stage. The time-constant of the feedback loop is sufficiently long to prevent any limiting of the low duty-cycle picture highlights.

Luminance Stage Performance

The bandwidth of the PL802 stage is 5MHz at −3dB, which is quite adequate for a dual-standard receiver. It is advisable to use a subcarrier trap circuit in the luminance chain at some convenient point to reduce the gain at 4·43MHz by some 3 to 4dB. This reduces the radiation of the subcarrier from the luminance stage and also reduces the visibility of the subcarrier pattern on the picture.

The voltage gain of the amplifier is approximately 35 times, allowing full drive (100V black-white) to be obtained with a 3V black-white detector signal.

SYNCHRONISING PULSE SEPARATOR AND LINE OSCILLATOR

The synchronising pulse separator and line oscillator in a colour receiver perform similar functions to their counterparts in a monochrome receiver. The separator is driven from a low-level signal source, and a transistor is used for the separator.

Circuit Description

The synchronising pulse separator and line oscillator circuit are shown in Fig. 4. A BC107 transistor, TR_{15}, is employed as the separator, operating with a collector potential derived from the 220V line. This enables a synchronising waveform to be obtained directly from the separator transistor having sufficient amplitude to drive the flywheel phase detector and field separator.

A composite video waveform of 5V peak-to-peak amplitude is developed across the collector resistor R_{307} (Fig. 1) of the second luminance phase splitter transistor TR_{12} to drive the synchronising pulse separator. The stray capacitance at the emitter due to the screened wiring to the contrast control RV_{302} causes h.f. overshoot at the collector. Compensation for this effect is provided by the shunt capacitor C_{303} in the collector circuit.

The collector waveform of the splitter transistor is taken to the base of the separator TR_{15} via a long-time-constant a.c. coupling C_{316}, R_{339} which, because of the base current flowing during the synchronising pulse tips, reverse-biases the base of the separator in the conventional way. Resistor R_{338} supplies a small forward-bias current to ensure that the separator collector bottoms satisfactorily during the synchronising pulse tips with video signals having a low average level. A low forward impedance diode D_{308} is included in the emitter circuit to safeguard the transistor against base-emitter breakdown due to surges caused by abnormal operating conditions.

A transformer T_{301} with a resonant secondary circuit, L_{304}, C_{317}, is connected in the lower part of the collector potential divider network. This produces a damped sine-

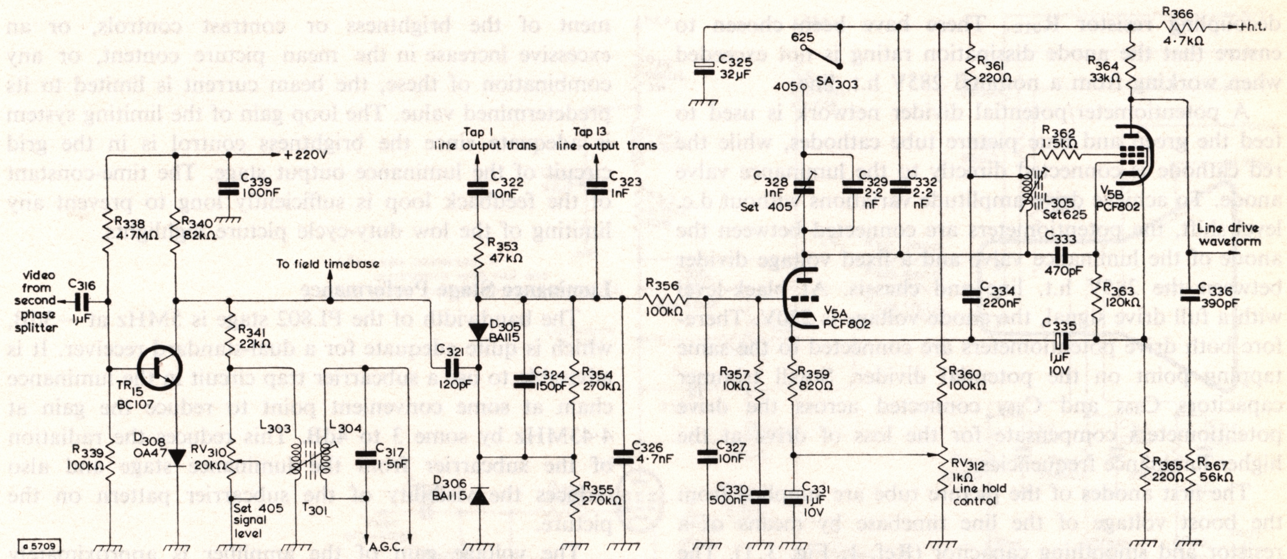
video from second phase splitter
C316 1μF
R338 4·7MΩ
R340 82kΩ
C339 100nF
+220V
TR15 BC107
R339 100kΩ
D308 OA47
RV310 20kΩ
Set 405 signal level
R341 22kΩ
L303
L304
T301
C317 1·5nF
A.G.C.
To field timebase
Tap 1 line output trans
Tap 13 line output trans
C322 10nF
C323 1nF
R353 47kΩ
D305 BA115
D306 BA115
C321 120pF
C324 150pF
R354 270kΩ
R355 270kΩ
C326 4·7nF
R356 100kΩ
C325 32μF
625
405
SA303
C328 1nF Set 405
C329 2·2 nF
C332 2·2 nF
V5A PCF802
R357 10kΩ
C327 10nF
C330 500nF
R359 820Ω
C331 1μF 10V
R360 100kΩ
RV312 1kΩ Line hold control
R361 220Ω
C334 220nF
R362 1·5kΩ
L305 Set625
C333 470pF
C335 1μF 10V
R363 120kΩ
V5B PCF802
R364 33kΩ
R366 4·7kΩ
+h.t.
Line drive waveform
C336 390pF
R365 220Ω
R367 56kΩ
a5709

Fig. 4—Line oscillator and synchronising pulse separator circuits

wave initiated by the line synchronising pulse which is used in the a.g.c. circuit for 405-line operation.

The pentode section of the PCF802 operates as a screen-coupled Hartley oscillator with the line drive developed at its anode. The triode section of the valve functions as a variable capacitive reactance element. A quadrature sinewave which is developed across the resistor R_{361} connected in series with the tuned-circuit inductor L_{305} is applied to the triode cathode via C_{334}. In addition to this, a feedback waveform with a predominantly anti-phase component is applied to the triode cathode via C_{335} from the pentode cathode network. This is positive feedback. It produces a negative-resistance component in the anode impedance of the triode which reduces the damping on the oscillator tuned circuit and ensures adequate sinewave drive to the pentode. This is important for preserving a fast negative edge to the line drive waveform developed at the pentode anode.

System switching is carried out by a single switch contact SA_{303} which places additional capacitance (C_{328} and C_{329}) across the tuned circuit for 405-line operation. The line hold control RV_{312} varies the d.c. bias of the triode over a limited range. The inductor L_{305} is the preset adjustment for 625-line operation, and C_{328} the adjustment for 405-line operation.

The double-diode phase detector is driven via C_{321} from the collector of the synchronising pulse separator. The coupling capacitor, C_{321}, is kept to a low value to minimise the field pulse group disturbance in the flywheel system, which may otherwise appear as a horizontal displacement at the top of the picture, and also to reduce the sensitivity of the flywheel to low-frequency noise or interference on the incoming signal. A sawtooth phase-reference waveform having an amplitude of approximately 25V peak-to-peak is developed by integration (R_{353}, C_{326}) of a flyback pulse of approximately 600V peak amplitude obtained from a tap on the line output transformer. The phase detector should operate with an output potential of nominally zero volts at phase centre. To obtain this condition the negative-going edge of the sawtooth reference waveform developed across the integrating capacitor C_{326} must be speeded up. This is achieved by adding a negative-going pulse obtained from a separate winding of the line output transformer via capacitor C_{323}. This is preferable to using a phasing capacitor across the integrating resistor R_{353} which could introduce large-amplitude pulses into the phase detector circuit as a result of picture-tube flashover.

This simple form of phase detector has the disadvantage that, in the absence of the synchronising waveform, diode rectification of the sawtooth waveform occurs through D_{305} and C_{321}, and results in a small residual positive charge on C_{321} which appears, via R_{354}, at the output of the phase detector. This has the effect of sending the line oscillator off its correct frequency, and consequently the pull-in range is not situated symmetrically about the centre frequency. This imbalance can be reduced by keeping C_{321} to a low value; further reduction of imbalance can be achieved by connecting a small capacitor C_{324} across diode D_{305}. The diode is caused to conduct by the reference waveform, and a charge is produced on C_{324} which opposes the charge on C_{321}. By a suitable proportioning of C_{324} and C_{321}, the residual imbalance can be reduced appreciably.

The oscillator is set up by first setting the line hold control to the centre of its range, adjusting L_{305} for 15·625kHz and then, after changing the system switch, adjusting C_{328} for 10·125kHz.

Typical performance figures for the oscillator are as follows:

	625-line	405-line	
Oscillator control sensitivity	400	200	Hz/V
Pull-in range	800	400	Hz
Mains stability (h.t. plus heaters)			
+10%	−5	−10	Hz
−10%	+5	+10	Hz
Drive waveform fall time	1	1	μs

A.G.C. REQUIREMENTS

The automatic gain control requirements for the dual-standard i.f. amplifier described in Ref. 2 are determined by the control characteristics of the first i.f. transistor (BF167) and the tuner r.f. transistor (BF180).

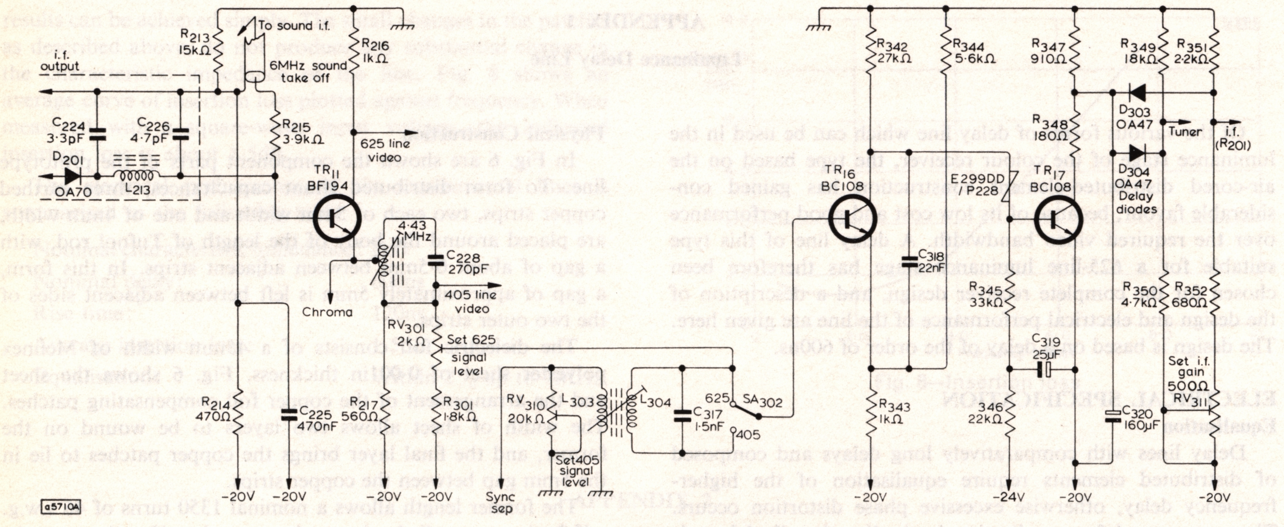
i.f. output
R213 15kΩ
To sound i.f.
6MHz sound take off
R216 1kΩ
C224 3·3pF
C226 4·7pF
D201 OA70
L213
R215 3·9kΩ
625 line video
TR11 BF194
4·43 MHz
C228 270pF
405 line video
Chroma
RV301 2kΩ
Set 625 signal level
R214 470Ω
C225 470nF
R217 560Ω
R301 1·8kΩ
-20V
-20V
-20V
-20V
Sync sep
RV310 20kΩ
L303
L304
Set405 signal level
C317 1·5nF
625
SA302
405
R342 27kΩ
R344 5·6kΩ
TR16 BC108
C318 22nF
R343 1kΩ
-20V
R347 910Ω
R348 180Ω
E299DD /P228
TR17 BC108
R345 33kΩ
C319 25μF
346 22kΩ
-24V
-20V
R349 18kΩ
R351 2·2kΩ
D303 OA47
D304 OA47
Delay diodes
Tuner
i.f. (R201)
R350 4·7kΩ
R352 680Ω
Set i.f. gain 500Ω RV311
C320 160μF
-20V
a5710A

Fig. 5—A.G.C. circuit

The BF167 is operated over a current range of 4mA to 13mA to achieve approximately 30dB of forward gain control. The mode of operation is partly current control and partly voltage control, and calls for a low-impedance a.g.c. circuit. The limits of the control range are fixed by the correct choice of emitter resistor; the minimum base voltage (maximum gain) and the extent of bottoming (minimum gain) are set by a preset potentiometer. These circuit limits give an accurately defined range of i.f. control with different samples of i.f. transistor. The choice of operating conditions for the controlled transistor has been fully described by Gander *et al* (Ref. 2).

The BF180 has similar requirements, but the maximum control need not be defined; the major requirement being to ensure that the signal-handling ability is not impaired by too large an i.f. gain reduction before the transfer of control.

Synchronising pulse tip amplitude control is used for 625-line operation, employing a d.c. coupled system which works on a peak-detection principle when the receiver is on tune but a mean-level principle while tuning in. This system avoids the possibilities of lock-out which can occur in gated systems when running in an unsynchronised condition (that is, during tuning and system switching).

To achieve similar operation on the 405-line system, it is convenient to sample the back-porch amplitude for the black-level reference. It is also necessary to allow for mean-level operation during tuning and system switching. This is achieved in the present circuit by adding a constant-amplitude pulse to the detected (d.c. coupled) video signal, timed to coincide with the back-porch period. Such a pulse is obtained by a damped ringing circuit which is pulse-excited by the line pulse at the collector of the synchronising pulse separator. Because of the limiting action of the separator, a pulse of nearly constant amplitude is achieved over a wide range of signal strengths; any marginal variations are proportional to signal strength in the correct sense to reinforce the a.g.c. action. The ringing circuit is tuned to a period of approximately 16μs, so that the first positive overswing occurs during the back porch period on a 405-line signal. An advantage of this system is that system switching requires only a change-over switch which selects the direct video signal (625-line) or the video signal plus sampling pulse (405-line).

Circuit Description

The a.g.c. circuit is shown in Fig. 5. A proportion of the video signal at the emitter of the phase splitter TR_{11} is taken from the slider of the preset potentiometer RV_{301} to the base of TR_{16} either directly or via the pulsed ringing circuit L_{304}, C_{317}, according to the position of the system switch.

A reference bias is applied to the emitter of TR_{16} by the voltage divider R_{343}, R_{344}. When the d.c. detector output level exceeds this bias by about 0·6V, control begins. Alternatively, if the peak pulse (synchronising or additional) of a received signal exceeds the reference bias, the transistor draws pulses of current which are smoothed and coupled to the output stage TR_{17}. The inclusion of the smoothing capacitor C_{318} allows the transistor to draw high peak currents without bottoming. The level at which a.g.c. action starts is set by adjustment of RV_{301}, which controls the proportion of video signal applied to the a.g.c. circuit.

The a.g.c. control transistor TR_{17} is d.c. coupled to TR_{16} by a voltage dependent resistor chain. The collector circuit of TR_{17} is coupled to the tuner and i.f. circuits by the two delay diodes D_{303} and D_{304}, which determine the range of control for the i.f. and r.f. amplifiers.

At low signal inputs, TR_{17} is conducting heavily, maintaining D_{303} in conduction, which in turn causes the base voltage of the first i.f. transistor to be held at a low value (that is, in the high gain condition). As the signal increases in value, TR_{17} conducts less, as does D_{303}. This allows the base voltage of the first i.f. transistor to rise, reducing the i.f. gain. This action continues until D_{303} is completely cut off by the voltage difference between the collector of TR_{17} and the preset (minimum gain) potentiometer RV_{311}, and R_{352} in the base circuit of the first i.f. transistor. Further reduction of current in TR_{17} due to an increase in signal strength causes diode D_{304} to conduct, thus raising the base voltage of the tuner r.f. transistor and reducing the overall tuner gain.

APPENDIX 1

Luminance Delay Line

Of the various forms of delay line which can be used in the luminance stage of the colour receiver, the type based on the air-cored distributed-element construction has gained considerable favour, because of its low cost and good performance over the required video bandwidth. A delay line of this type suitable for a 625-line luminance stage has therefore been chosen for the complete receiver design, and a description of the design and electrical performance of the line are given here. The design is based on a delay of the order of 600ns.

ELECTRICAL SPECIFICATION

Equalisation

Delay lines with comparatively long delays and composed of distributed elements require equalisation of the higher-frequency delay, otherwise excessive phase distortion occurs. The system used for equalisation in the line described here is based on work by Kallmann (Ref. 3). It consists of a row of copper strips or 'patches' extending the entire length of the delay line. These copper patches are electrically floating and become bridging capacitances, which compensate for the effective loss of inductance in the line at the higher frequencies. By careful adjustment of the size of the patches, delay equalisation within one to two per cent can be achieved over a wide frequency range.

Characteristic Impedance

The delay per unit length of delay line decreases as the impedance of the line increases. The impedance is a compromise between such factors as the ease of termination, drive requirement, and physical size. A value of 1kΩ has been chosen here as a good compromise between drive requirements and external termination effects. When a driver transistor is used at the input to the line, a signal power of about 10mW is required at the collector to produce subsequent full drive for the picture tube, yet (as shown in Fig. 7) only a very minor change is made in the delay line performance when the end of the line is shunted with a 33pF capacitor to represent the input of the following video stage. In addition, a 1kΩ delay line can be reasonably short (about 105mm) and it can have a small insertion loss.

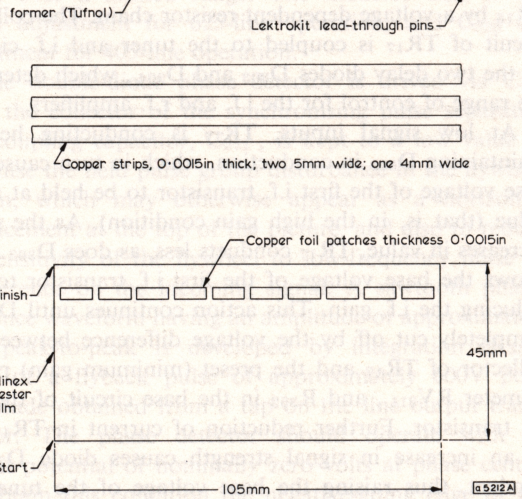
105mm
¼in former (Tufnol)
Lektrokit lead-through pins
Copper strips, 0·0015in thick; two 5mm wide; one 4mm wide
Copper foil patches thickness 0·0015in
Finish
45mm
Melinex polyester film
Start
105mm
a5212A

Fig. 6—Constructional details of delay line

Physical Construction

In Fig. 6 are shown the component parts of the prototype line. To form distributed shunt capacitances, three earthed copper strips, two each of 5mm width and one of 4mm width, are placed around the body of the length of Tufnol rod, with a gap of about 0·5mm between adjacent strips. In this form, a gap of approximately 5mm is left between adjacent sides of the two outer strips.

The dielectric foil consists of a 45mm width of Melinex polyester sheet of 0·001in thickness. Fig. 6 shows the sheet and the arrangement of the copper foil compensating patches. The width of sheet allows two layers to be wound on the former, and the final layer brings the copper patches to lie in the 5mm gap between the copper strips.

The former length allows a nominal 1350 turns of 46 s.w.g. self-fluxing enamelled wire to be wound uniformly over the dielectric foil. Lead-through pins provide suitable terminal points at each end of the former. In quantity, a printed plastic film would simplify fabrication and give very consistent results.

Electrical Performance

In Fig. 7, the variations of delay with frequency are shown for two sample sets of patches. Curves (a) and (b) were determined with a line containing a row of ten patches, 3·0×9·0mm, and curve (c) shows the performance of a line with twelve patches, 8·0×3·5mm. The figures show how the lines can be equalised by these single rows of patches to within two per cent up to about 6 to 7MHz. Curve (d) shows the typical performance of an uncompensated line, and indicates the excessive phase distortion without compensation.

Applying a step waveform of moderate rise time (not greater than 20ns) at the input of the lines produces a smoothly rising output waveform, substantially free from pre-shoot or overshoot. The measured rise time of both samples was about 120ns.

The two examples show that it is useful to experiment with small variations in the number and size of patches along the line before a final choice is made, because of the empirical nature of the fine adjustment of delay equalisation. Once the number and size of patches along the line are decided, repeatable results can be achieved simply. The small changes in the patches as described above, do not produce any substantial change in the characteristic impedance of the line. Fig. 8 shows an average curve of insertion loss plotted against frequency. When measured with a square-wave input voltage, the indicated insertion loss is about 1·5dB.

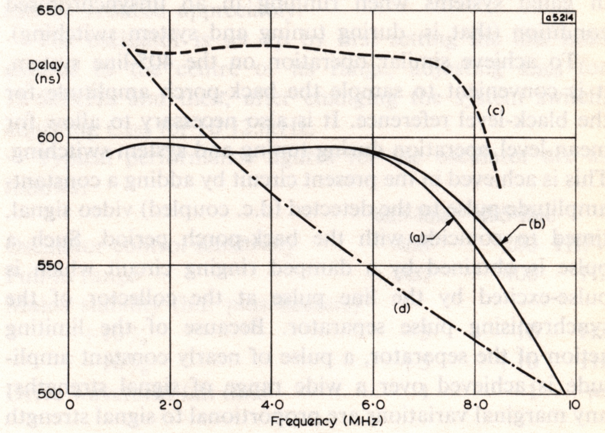

Fig. 7—Delay characteristics for:
(a) Delay line containing 10 patches, 9×3mm
(b) Delay line (a) with 33pF capacitor at end of line
(c) Delay line containing 12 patches, 8×3·5mm
(d) Unequalised delay line

The electrical performance of the experimental lines is summarised in the following table:

Nominal characteristic impedance:	1kΩ
Nominal delay:	600ns
Rise time:	120ns
Average insertion loss:	1·5dB
Equalisation:	Within 2% up to 7MHz.

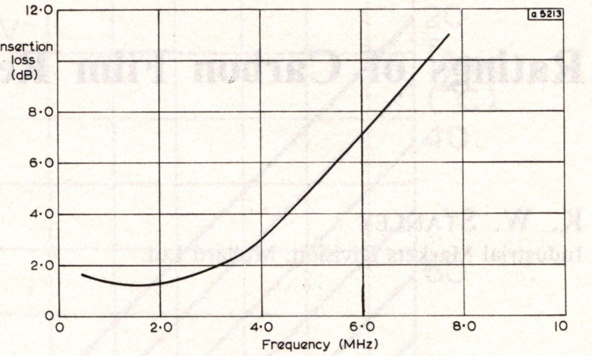

Fig. 8—Insertion loss

APPENDIX 2

Grey-scale and Colour-difference Adjustments

GREY-SCALE ADJUSTMENTS

To obtain good grey-scale operation, it is necessary to adjust the drive conditions of the three electron guns carefully for each individual picture tube. Grey-scale tracking is obtained initially by setting the cut-off voltage of each electron gun to the same value and then adjusting the luminance drive to obtain the correct white point. A grid cut-off voltage of −110V is chosen so that the rated beam current can always be obtained. Since the picture-tube cathodes are directly coupled to the luminance stage, their black-level voltage (cut-off) point is fixed at +220V. Therefore the grid clamps are returned to +110V giving a −110V setting for cut-off.

Adjustment is carried out by setting the anode voltage of the luminance output stage at +220V on a blank raster by means of the brightness control and then varying the first anode potentials by means of the three preset potentiometers, RV_{305}, RV_{306}, RV_{307} in Fig. 2. Switches S_B, S_C, and S_D for the three guns facilitate the separate adjustment of the three potentials.

The cut-off values having been set, the drives applied to the blue and green guns are adjusted for a good peak white colour on a step-wedge test pattern. A further slight adjustment may be made, if necessary, to improve the colour neutrality in the dark grey region. This must be followed by a final adjustment of the luminance drives for white.

For a correct grey-scale with cathode drive, taking into account picture spreads, the ranges of full drive voltage required when the cut-off voltages are set to −110V are:

Red cathode	100V to 87V
Blue cathode	94V to 74V
Green cathode	96V to 76V.

COLOUR-DIFFERENCE DRIVE ADJUSTMENT

Colour-difference adjustments are best carried out by reference to a colour-bar signal displayed on the picture tube. Initially, the contrast control is set to about 80% maximum; with the blue and green guns switched off, the chrominance preset saturation control is adjusted until the two pairs of red bars are of equal brightness. When this relative setting of contrast and chrominance saturation is achieved, the blue colour-difference drive is adjusted with the red and green guns turned off so that bars of equal brightness are obtained.

Finally, the green drive is adjusted to cancel the luminance graduation on the bright and dark halves of the green gun picture. These comparatively subjective adjustments, using the visual output of the picture tube, give quite consistent results and require very short setting-up times.

COIL AND TRANSFORMER SPECIFICATION

L_{305} (Fig. 4)	2000 turns, 42 s.w.g. e.s.s. tapped at 500 turns quarter wavewound ⅝in wide Former: Aladdin short ¼in dia. Magnetic slug: FX1068.
L_{303}/L_{304} (Figs. 4 and 5)	Primary: 600 turns, 40 s.w.g. en.cu., silk covered, wavewound 6mm wide. Secondary: 300 turns, 40 s.w.g. en.cu., silk covered, wavewound 6mm wide. Space between windings: 2mm Former: ¼in dia. S.R.B.P. tube Magnetic slug: FX1068, fully inserted
L_{213} (Fig. 5)	75 turns, 44 s.w.g. en.cu. wire on dust iron former, Neosid CH2.

REFERENCES

1. **LAMMERS, J., and SKELTON, D.** 'Shunt-stabilised Line Timebase'. **Mullard Technical Communications,** Vol. 9, No. 83, Sept. 1966, pp. 69 to 72.
2. **GANDER, M. C., HEINS, H. A., and HOBBS, D. S.** 'A.G.C. for Monochrome and Colour Receivers'. **Mullard Technical Communications,** Vol. 9, No. 85, Jan. 1967, pp. 119 to 124.
3. **KALLMANN, H. E.,** 'Equalized Delay Lines'. **Proc. I.R.E.,** Vol. 34, Sept. 1946, pp. 646 to 657.

Ratings of Carbon Film Resistors

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Nomograms relating electrical dissipation, ambient temperature, body temperature, resistance value, stability, and the physical dimensions of resistors are given. They allow a rational and economic choice of resistor type to be made for given electrical, temperature, and stability requirements. In suitable circumstances, resistors may be used at dissipations substantially in excess of their conventional power ratings. This approach leads to the abandonment of the classification of resistors as $\frac{1}{8}$W, $\frac{1}{4}$W, and so on, and to the adoption of classification by physical size.

INTRODUCTION

Despite the large numbers of fixed resistors used in conventional circuits, there is insufficient appreciation of the factors that should determine the choice of a resistor type for a particular set of conditions, or of the interrelationships of these factors. It is, for example, usual to regard the power rating of a resistor as an absolute limit, irrespective of the ambient temperature and the required stability. In this way, unnecessarily large resistors (in terms of power rating and physical dimensions) may be specified, and the equipment may be significantly larger and more expensive than it would have been if a more rational method of choice had been followed.

The ultimate determining factor in the choice of a resistor type is not its power rating but the maximum temperature attained during operation; that is, the "hot-spot" temperature, which normally occurs half-way between the ends of the resistor. The hot-spot temperature is a function of the electrical dissipation and of the ambient temperature; and it is a main determinant of the stability of the resistance value during life.

With data relating to resistors of various physical sizes, the circuit designer is able to specify resistors on the basis of the actual electrical dissipation and the stability that will be achieved. Within the appropriate temperature and voltage limits, stability and electrical dissipation can be traded one for the other; or, as the dissipation and stability are likely to be fixed requirements, the best physical size that will meet both requirements can be chosen. The maximum voltage rating of the resistor must be satisfied; but the supposedly mandatory wattage rating can be ignored. Further, high stability may be obtained with resistors from normal ranges.

RESISTOR STRUCTURE AND BEHAVIOUR

The two nomograms relate to the Mullard resistor ranges CR16 and CR25. The CR16 resistors have a body diameter of 1·6mm; and the CR25, of 2·5mm. These ranges will no longer be known as $\frac{1}{10}$W and $\frac{1}{8}$W resistors.

Both ranges are of carbon film type, except that values up to 10Ω in the CR25 range are made with a metal film.

Carbon Film Resistors

The carbon film resistor consists of a cylindrical ceramic rod onto which a carbon film is deposited. The resistor is completed by addition of end-caps, protective lacquer coatings, and code-marking. To produce a range of resistance values, a helical track is cut in the film. By control of the film thickness and the effective length and width of carbon track between the terminals, a large range of resistance values can be obtained with reasonable component sizes.

Behaviour during Life

A voltage limit is imposed to protect the resistor from electrical breakdown across the turns of the helix or through the insulating lacquer. Observation of this limit enables the inherently very high reliability of carbon film resistors to be achieved. A failure rate of better than 0·0002%/1000h is typical for the most widely used values of resistor.

Disregard of the hot-spot temperature limit can lead to catastrophic failure caused by the protective lacquer lifting from the ceramic rod and pulling away sections of the carbon film. It will, also, certainly reduce the stability of the resistance value.

Life tests have shown that, for conditions within the specified voltage and temperature limits, significant changes in resistance will be substantially complete well within the first 1000 hours. Later changes will be relatively slight. It is therefore reasonable to quote the maximum expected drift of resistance value as

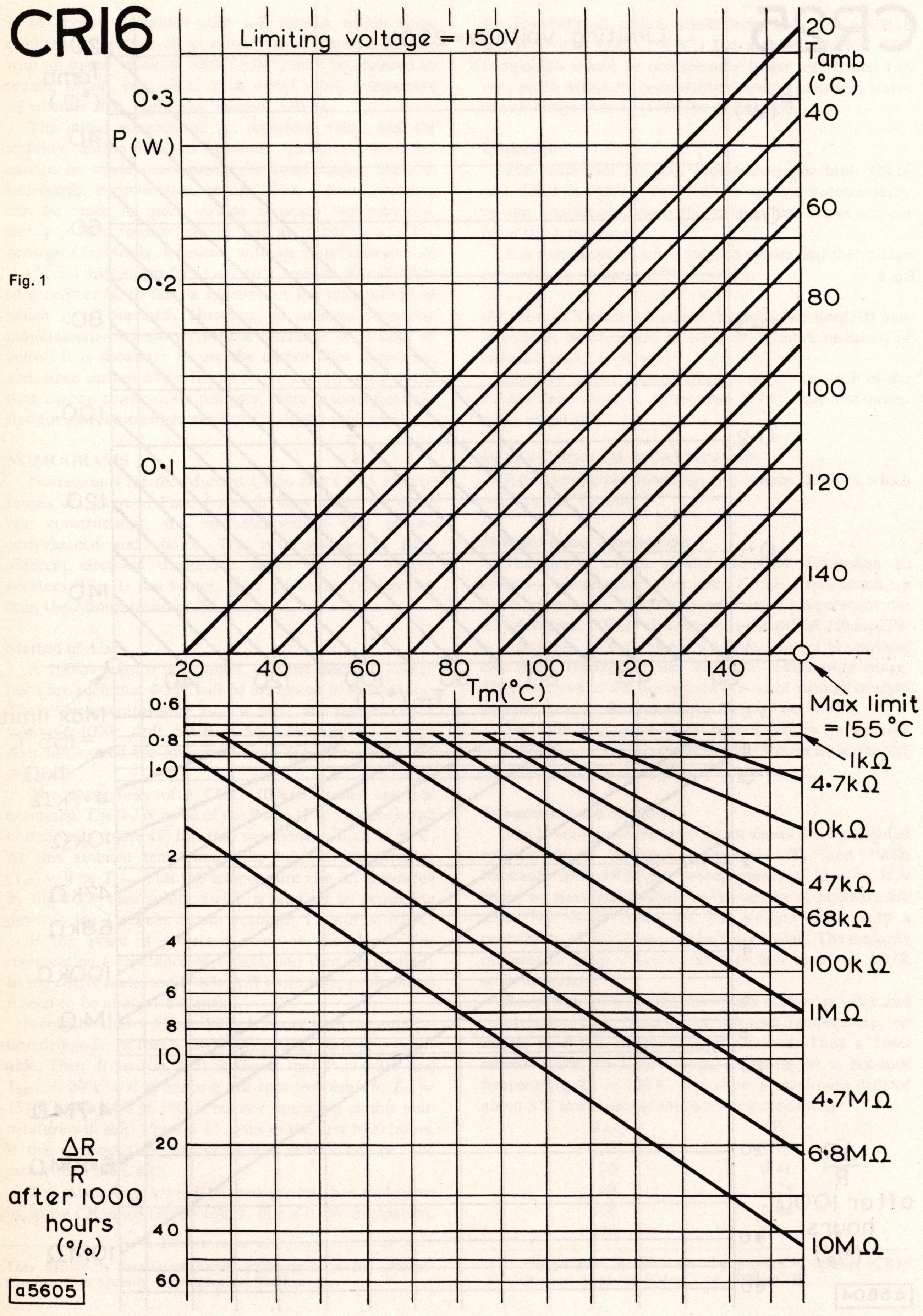
$$\frac{\Delta R}{R}\%/1000\text{h}$$

with a probability of 95%.

Accuracy and Stability

When a fixed resistor is to be specified, its voltage and current conditions will be known. Thus a resistor with a particular resistance value will be required. The nature of the application will determine the limits that must be placed on this initial value, and on the drift that will be tolerable during life. A resistor with, say, ±10% tolerance on its nominal initial value will be specified. The next step

Fig. 1



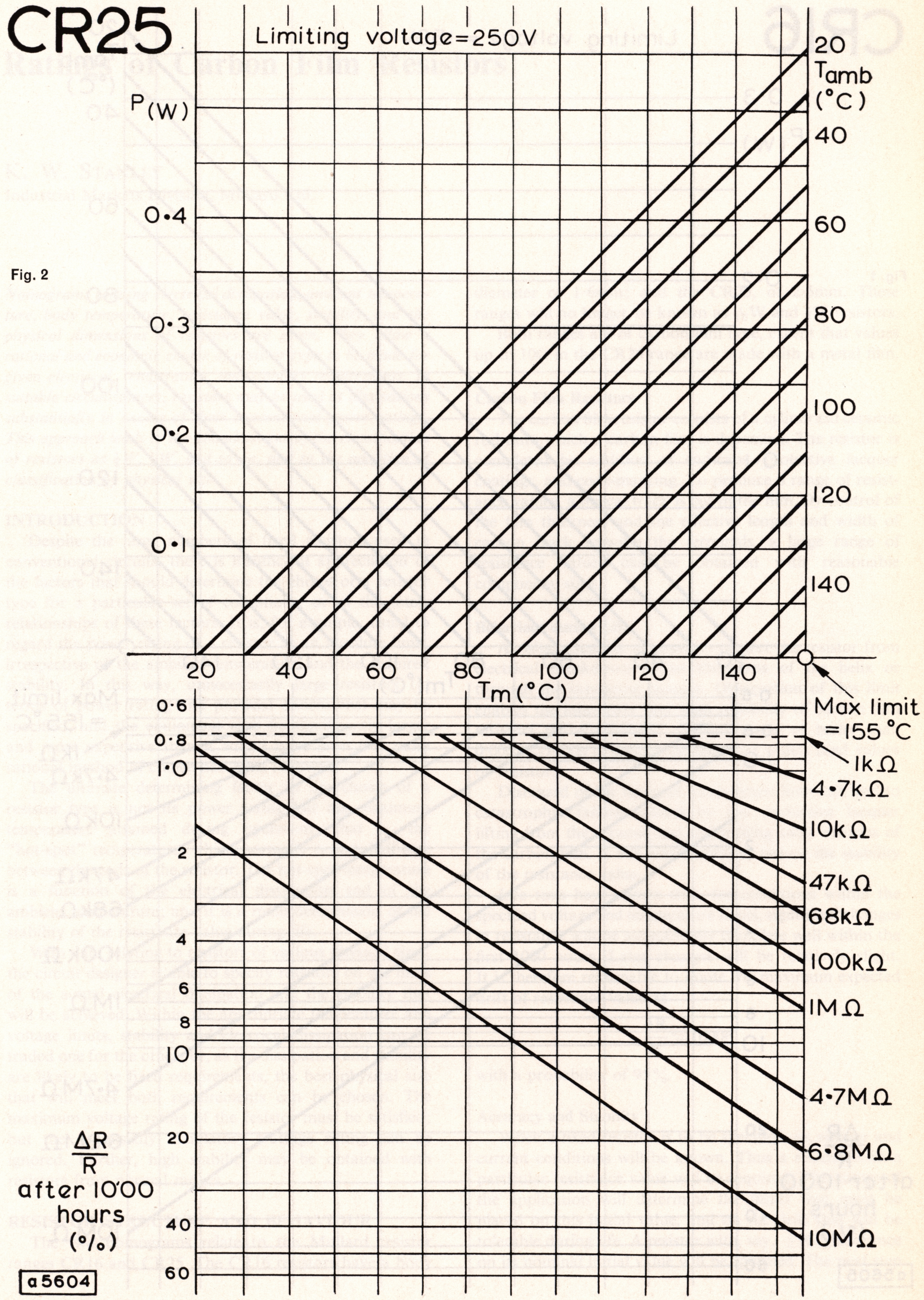


Fig. 2

is to choose a resistor that will remain within some required percentage of its initial value. Thus, a resistor with an initial value of 100kΩ±10% may be required to remain within, say, ±4% of its initial value, irrespective of whether that value was 90kΩ or 110kΩ.

The initial accuracy of the resistance value, and the stability during life, are separate questions. Resistors cannot be made economically to exact values; there is necessarily a production spread (from which selections can be made to meet various accuracy requirements). But a −10% resistor can be just as stable as a −1% resistor. Conversely, a resistor with an initial tolerance of ±1% can drift just as far as a ±10% resistor. The stability of a resistor is, in fact, a function of the temperature at which it is operated. However, to achieve economic manufacture of resistors with a tolerance of ±10% or better, it is necessary to use the carbon film technique; and, since carbon film resistors are inherently more stable than carbon composition resistors, there is some justification for associating high stability with high initial accuracy.

NOMOGRAMS

Nomograms for the Mullard CR16 and CR25 resistor ranges are given in Figs. 1 and 2. They show, for these two constructions, the interrelationships that govern performance and choice. The two nomograms have different electrical dissipation scales (P). The 1·6mm resistors (Fig. 1) run hotter, for a particular dissipation, than the 2·5mm resistors (Fig. 2).

Method of Use

A 100kΩ resistor is required, and the electrical conditions are such that 0·3W will be dissipated in the resistor. The ambient temperature T_{amb} is 30°C, and the maximum tolerable 1000h drift ΔR/R is 5%. The applied voltage does not exceed the maximum limit for either the CR16 or CR25.

The possibilities of a CR25 100kΩ resistor are first examined. The 0·3W point of the P axis (Fig. 2) is projected horizontally to the 45° line that represents a T_{amb} of 30°C. At this ambient temperature the hot-spot temperature (T_m) will be T_{amb} plus the temperature rise ΔT produced by the 0·3W dissipation; and it is read off by projecting down to the T_m scale. In our example, T_m will be 103°C.

If this point is projected down to the sloped line representing a resistance of 100kΩ, and then horizontally to the ΔR/R scale, the 1000h drift (with 95% probability) is seen to be about 1·5% max.

It may be that 1·5% stability is better than the application demands; or that a physically smaller resistor is desirable. Then, from Fig. 1, it is found that P = 0·3W and T_{amb} = 30°C will produce a hot-spot temperature T_m = 151°C; and a CR16 100kΩ resistor operating at this temperature will drift about 4·1% max in the first 1000 hours. If this is acceptable, then the CR16 resistor can be used rather than the CR25.

The saving in space will be even greater than that given by using CR16 instead of CR25. For a 0·3W dissipation, the conventional choice would have been not a CR16 (“$\frac{1}{10}$W”) or a CR25 (“$\frac{1}{8}$W”) but a 0·5W resistor. This component would be considerably larger and (being run very much within its potentialities) quite excessively stable (much better than 1%) for the application.

Limitations

The maximum hot-spot temperature for both CR16 and CR25 is 155°C. This limit is applied automatically by the nomograms, since the temperature scales are cut off at this temperature.

It is important, as a first step, to ensure that the voltage present is not excessive. Thus, where

$$P = V \times I$$

the value of V must not exceed the published limit. (It may sometimes be necessary to use two or more resistors, of reduced value, in series.)

Stability values derived from upward extension of the resistor lines (that is, better than 0·75%) are not necessarily achievable.

DERIVATION OF NOMOGRAMS

Each nomogram comprises two graphs, both of which relate to the T_m axis.

Dissipation and Temperature

The upper section relates electrical dissipation to hot-spot temperature. For the CR25 construction, a 0·2W increase in dissipation produces a temperature rise ΔT of 50degC*. This “dissipation constant” of 250degC/W is a function of the resistor structure, and it is constant and linear throughout the allowable temperature range. Thus this part of the nomogram is a set of parallel straight lines at an angle determined by $T_m = T_{amb} + \Delta T$.

The limit $T_{m(max)}$ = 155°C means that, in the extreme case of T_{amb} = 155°C, the allowable temperature rise ΔT (and therefore the dissipation P) must be nil.

Temperature and Stability

The lower part of the nomogram shows the exponential relationship of hot-spot temperature T_m and 1000h resistance drift ΔR/R for various values of resistor. It is based on statistical analysis of the results of extensive life tests. The ΔR/R values are the greatest drifts (with a probability of 95%) that will be experienced. The majority of resistors from a batch will drift less than the ΔR/R scale indicates.

Resistance drift, in resistors of any particular value and construction, is a function of hot-spot temperature, no matter how this temperature is attained. Thus a 1MΩ resistor from the CR25 range, operating at a hot-spot temperature T_m = 120°C, will show a maximum drift of about 3% under any of the following conditions:

T_{amb} (°C)	P (W)
20	0·41
60	0·25
100	0·08
120	0

This article is based on work performed in the Philips' Components Quality Laboratories, Eindhoven.

*The comparable increase for the physically smaller CR16 construction is about 80degC, or 400degC/W.

These sample operating conditions, it is worth noting, are for a resistor that was conventionally rated at P = 0·125W.

Resistance drift ΔR/R at a given temperature is determined, mainly, by the thickness of the carbon film. For a given body size, the lower value resistors give a better stability than the higher values. Thus, a 10MΩ resistor from the CR25 range, operating at (say) a hot-spot temperature of 90°C, has a probable maximum drift of 9%; while 1MΩ or 100kΩ resistors, from the same range and at the same temperature, will have drifts of about 1·7% and 1·1% respectively.

A thin carbon film (that is, with a higher resistance) is less stable, at any particular temperature, than a thicker carbon film. But the helical groove has different configurations for different resistance values. For this reason the lines relating to different resistances are neither parallel nor spaced in a strictly linear or logarithmic fashion. Interpolations for intermediate values will be approximate.

Other Factors

The life tests on which the drift values are based were performed on complete production spreads of resistors, including (for each value and type of resistor) samples with initial values extending throughout the appropriate tolerances. A −10% resistor will, in a life test that has been set up to provide a particular dissipation in nominal resistors, in fact run at a higher dissipation; while a +10% resistor will run correspondingly cooler and will drift less. These effects have been allowed for in the nomograms.

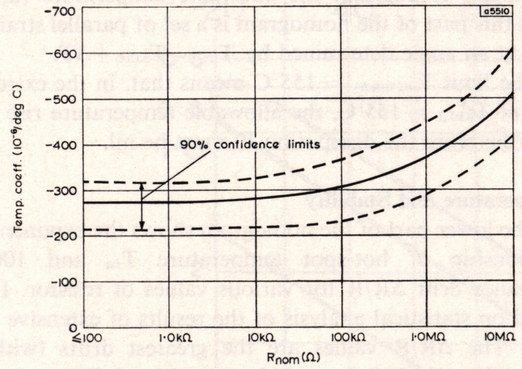


Fig. 3—Temperature coefficient as a function of the resistance value, for CR16 and CR25 ranges

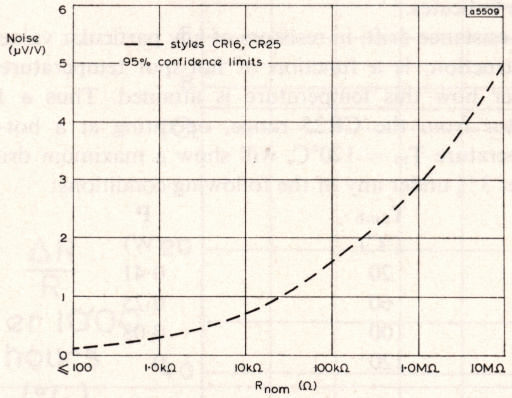


Fig. 4—Noise as a function of the resistance value, for CR16 and CR25 ranges

Voltage limitations have not been taken into account in the construction of the nomograms. If resistors from, say, the CR25 range, with resistance values from a few ohms to several megohms, are life tested, the observed drift will be greater for the higher value resistors. However, above a certain value of resistance it would be necessary to apply an excessive voltage to produce the higher levels of dissipation. Limitation of the voltage to the maximum permitted value would mean that the high-value resistors would be running at a lower dissipation than low-value resistors; and they would apparently be more stable. For the present ranges of resistors, and the operating conditions covered by the nomograms, the question is academic. Attention to the voltage and current conditions that are to be met, and the use of the actual dissipation value P that the resistors will have to withstand, will provide the correct answers from the nomograms.

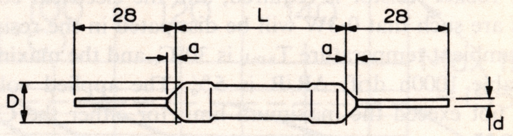
SUPPLEMENTARY INFORMATION

The two ranges of Mullard resistor are supplied in standard values from the E12 series. The resistance ranges covered are:

CR16 10Ω to 10MΩ ±10% tolerance
CR25 1Ω to 3·9Ω ±10% tolerance
4·7Ω to 1MΩ ±5% tolerance
*1·2MΩ to 10MΩ ±10% tolerance

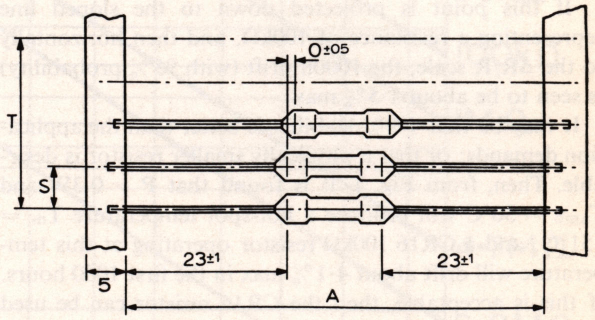
*Values between 1·2MΩ and 10MΩ will become available in the autumn of 1967.

The temperature coefficient for both ranges is shown in Fig. 3, and noise as a function of the resistance value in Fig. 4. Mechanical details are given in Figs. 5 and 6.



Type	D/dia max.	L_{max}	a_{max}	d/dia
CR16	1·6	6·5	0·5	0·4
CR25	2·5	8·5	0·5	0·6

Fig. 5—Dimensions (in mm). The dimensions 'L' and 'a' are measured from the point at which the resistor diameter is 0·8mm (CR16), 1·0mm (CR25)



style	A	S	T for number (n) of resistors	
			n<50	50<n<100
CR25	55±2	5 nom	5(n-1)±2	5(n-1)±4

Fig. 6—Positioning of CR25 resistors on tape (CR16 resistors are not supplied in this manner)